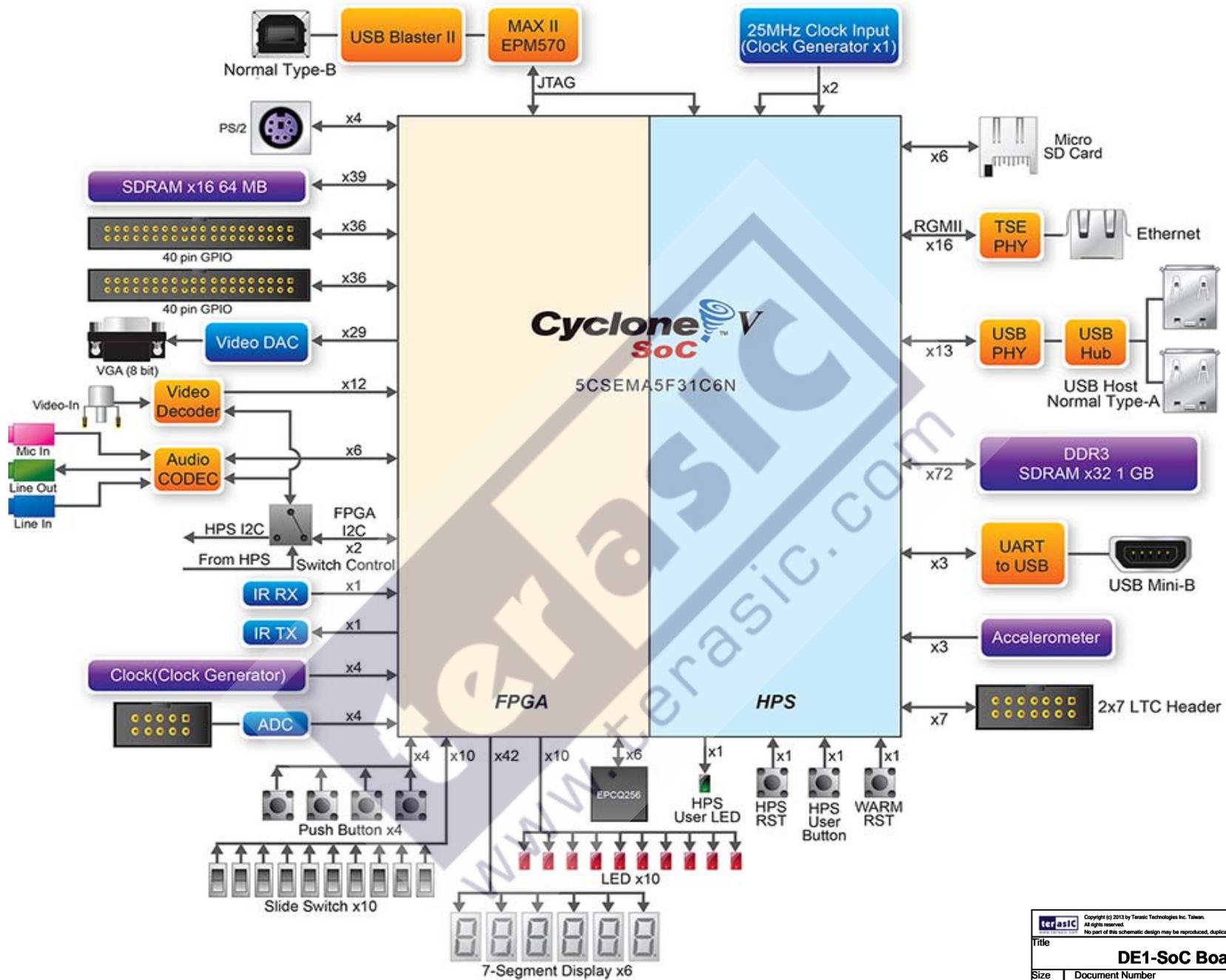


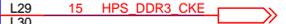
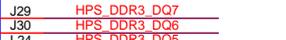
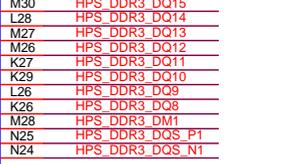
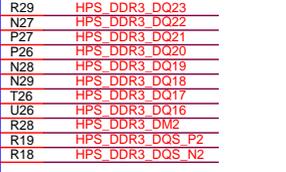
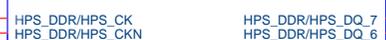
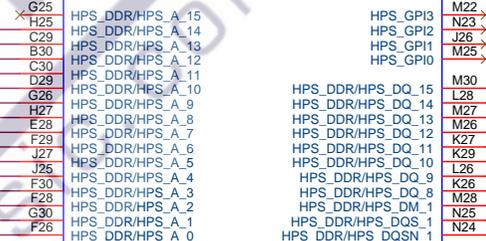
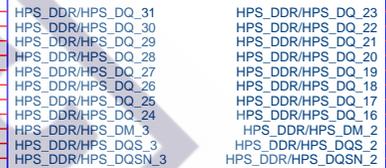
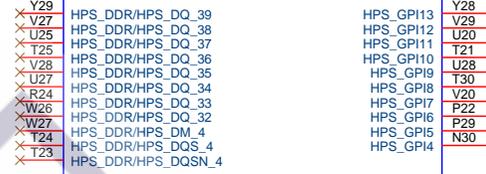
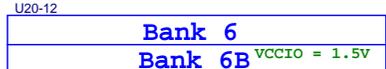
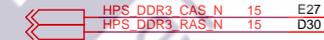
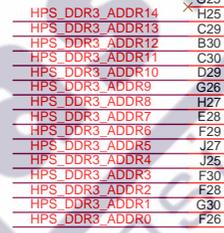
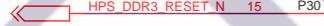
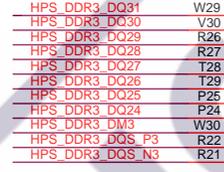
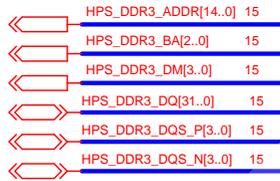
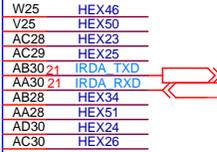
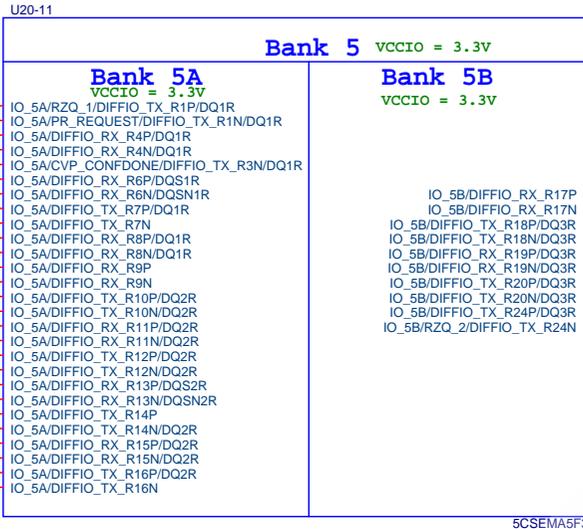
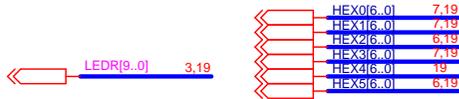
ALTERA Cyclone V SoC Development & Education Board (DE1-SoC)

| PAGE | CONTENT | PAGE | CONTENT |
|------|-----------------------|------|---|
| 1 | Cover Page | 16 | ADV7123 VGA |
| 2 | Block Diagram | 17 | ADV7180 Video Decoder |
| 3 | FPGA BANK 3, BANK 4 | 18 | Audio CODEC |
| 4 | FPGA BANK 5, BANK 6 | 19 | 7-Segment Display, LED |
| 5 | FPGA BANK 7, BANK 8 | 20 | FPGA BUTTON, Switch |
| 6 | FPGA Clocks, GND | 21 | ADC, PS2, IR Tx, IR Rx |
| 7 | FPGA Configuration | 22 | 2-port USB Host |
| 8 | FPGA Decoupling | 23 | 1 Gigabit Ethernet |
| 9 | FPGA Power | 24 | UART to USB, SD CARD |
| 10 | USB Blaster II | 25 | Accelerometer, LTC Connector |
| 11 | JTAG Chain | 26 | I2C Multiplexer, HPS BUTTON, HPS LED |
| 12 | GPIO 0 | 27 | Power - 1.1V |
| 13 | GPIO 1 | 28 | Power - 5V, 3.3V |
| 14 | SDRAM, HPS QSPI Flash | 29 | Power - 9V, 2.5V, 1.5V |
| 15 | HPS DDR3 SDRAM | 30 | Power - 1.2V, 1.8V, DDR3 VREF, DDR3 VTT |

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| Size | Document Number | Rev |
| B | Cover Page | E |
| Date: | Monday, October 20, 2014 | Sheet 1 of 30 |



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| Size | Document Number | Rev |
| B | Block Diagram | E |
| Date: | Monday, October 20, 2014 | Sheet 2 of 30 |

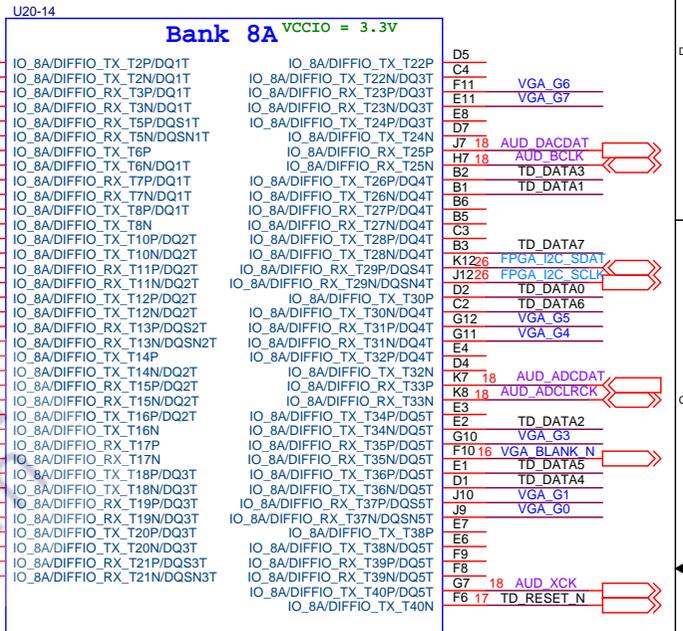
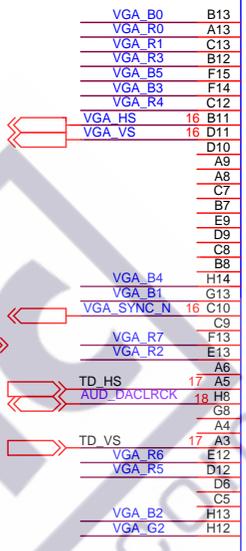
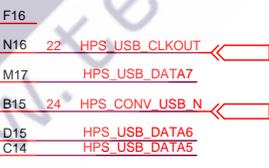
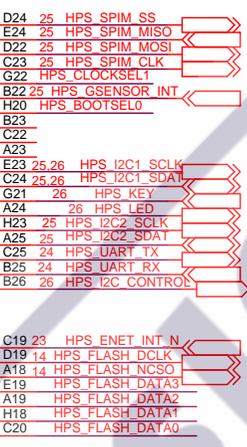
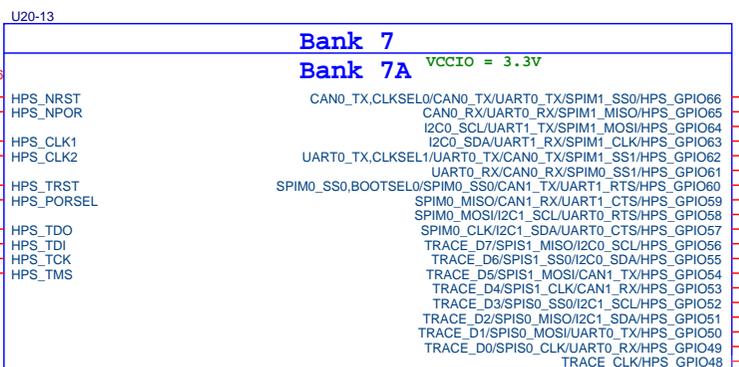
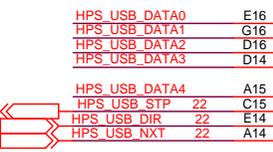
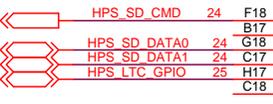
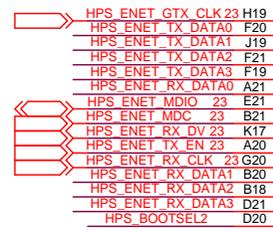
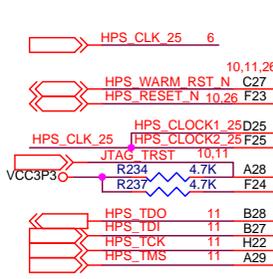
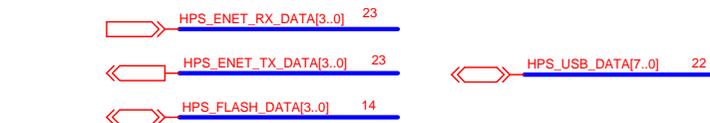


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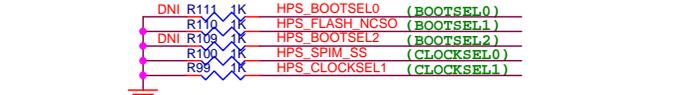
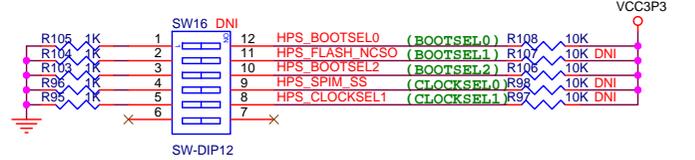
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Size B Document Number: **FPGA BANK 5, BANK 6** Rev E

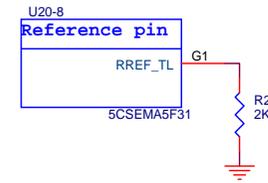
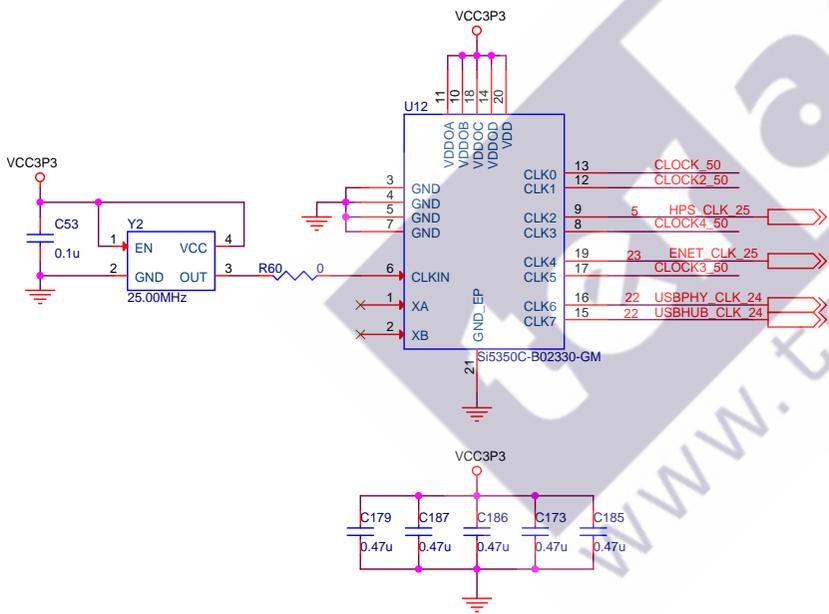
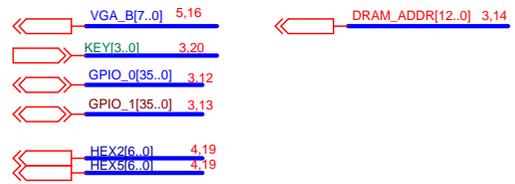
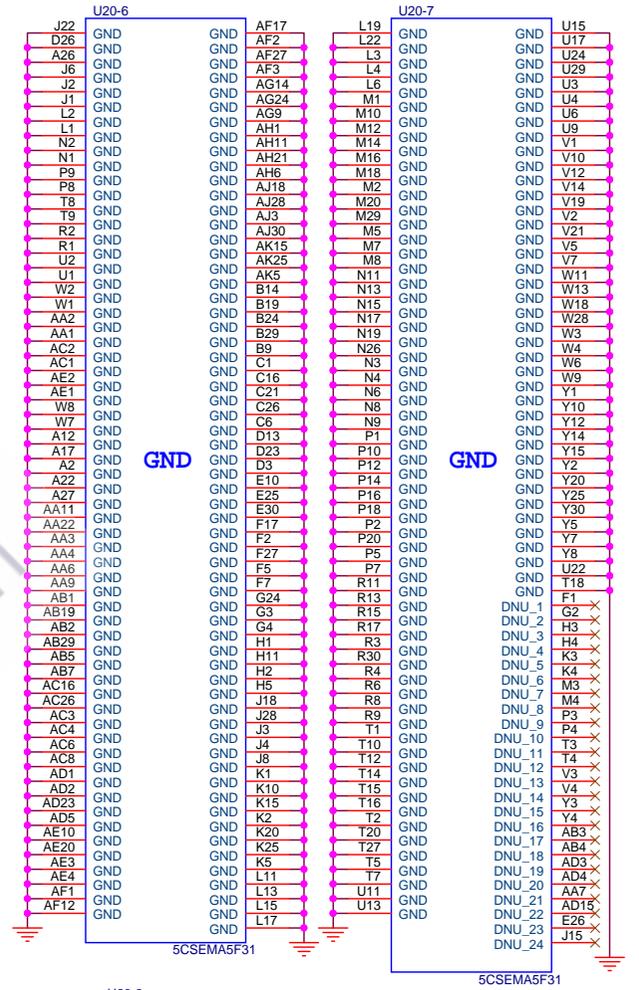
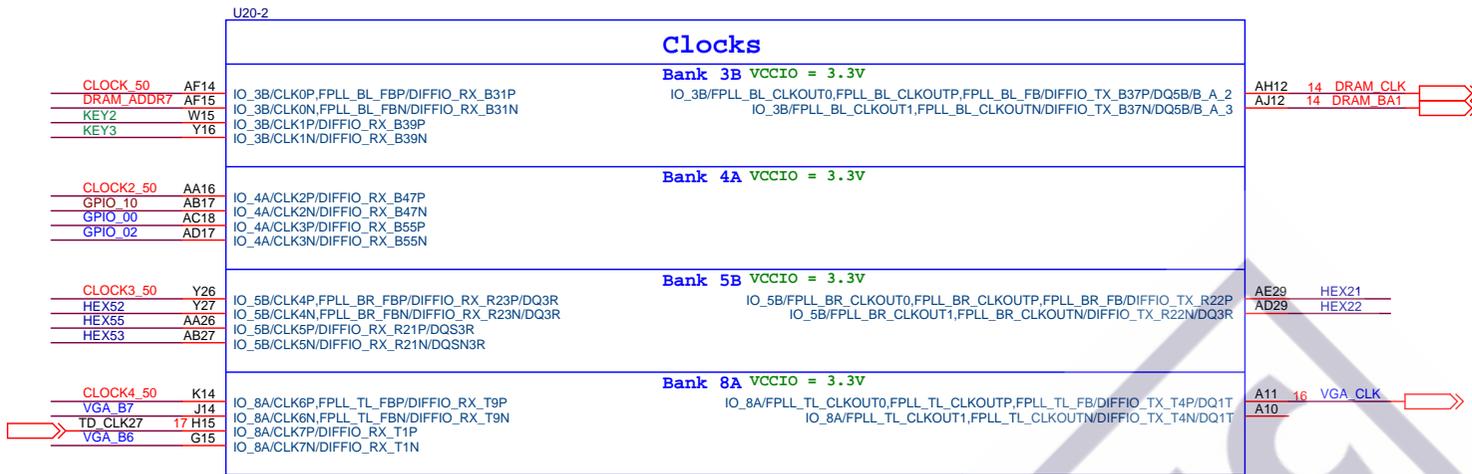
Date: **Monday, October 20, 2014** Sheet 4 of 30



Default Setting: BOOTSEL[2:0]=101 (Boot from SD CARD)
CLKSEL[1:0]=0



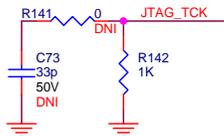
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| Title | | |
| DE1-SoC Board | | |
| Size | Document Number | Rev |
| B | FPGA BANK 7, BANK 8 | E |
| Date: | Monday, October 20, 2014 | Sheet 5 of 30 |



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| DE1-SoC Board | | | | | |
| Size | Document Number | | | | Rev |
| B | FPGA Clocks & GND | | | | E |
| Date: | Monday, October 20, 2014 | | | Sheet | 6 of 30 |

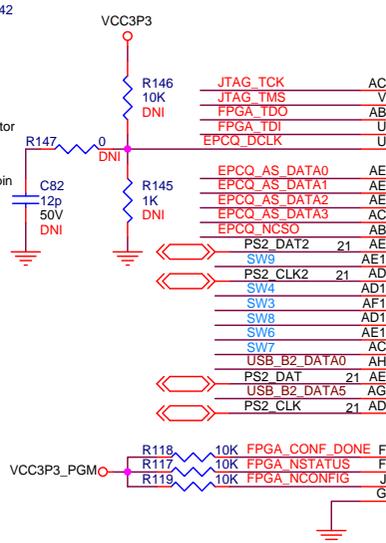
USB Blaster

- FPGA TDI 11
- JTAG TMS 11
- JTAG TCK 11
- FPGA TDO 11



Design Note:
Optional termination resistor for DCLK

CAD Note:
Place near FPGA DCLK pin



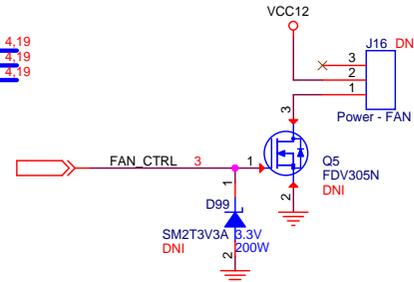
- FPGA NCONFIG 10
- FPGA_CONF_DONE 10

- USB_B2_DATA[7..0] 3,10
- SW[9..0] 3,20

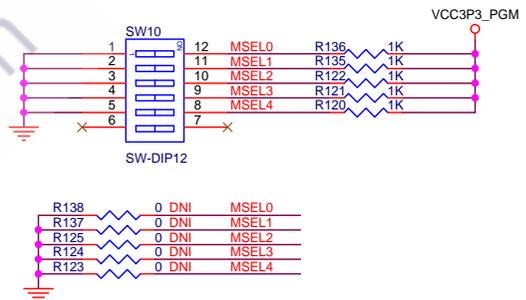
Configuration

| Bank 3A VCCIO = 3.3V | Bank 5A VCCIO = 3.3V |
|----------------------------------|----------------------|
| TCK | AD25 HEX32 |
| TMS | AC25 HEX33 |
| TDO | AE26 HEX00 |
| TDI | AJ29 HEX10 |
| DCLK | AD27 HEX16 |
| | |
| AS_DATA0/ASDO/DATA0 | |
| AS_DATA1/DATA1 | |
| AS_DATA2/DATA2 | |
| AS_DATA3/DATA3 | |
| NCSO/DATA4 | |
| IO_3A/DATA5/DIFFIO_TX_B2N | |
| IO_3A/DATA6/DIFFIO_RX_B1N/DQ1B | |
| IO_3A/DATA7/DIFFIO_TX_B2P/DQ1B | |
| IO_3A/DATA8/DIFFIO_RX_B1P/DQ1B | |
| IO_3A/DATA9/DIFFIO_TX_B4N/DQ1B | |
| IO_3A/DATA10/DIFFIO_RX_B3N/DQS1B | |
| IO_3A/DATA11/DIFFIO_TX_B4P | |
| IO_3A/DATA12/DIFFIO_RX_B3P/DQS1B | |
| IO_3A/DATA13/DIFFIO_TX_B6N/DQ1B | |
| IO_3A/DATA14/DIFFIO_RX_B5N/DQ1B | |
| IO_3A/DATA15/DIFFIO_TX_B6P/DQ1B | |
| IO_3A/CLKUSR/DIFFIO_RX_B5P/DQ1B | |
| | |
| Bank 9A | |
| CONF_DONE | L8 MSEL0 |
| NSTATUS | K6 MSEL1 |
| NCONFIG | G6 MSEL2 |
| NCE | L7 MSEL3 |
| | L9 MSEL4 |

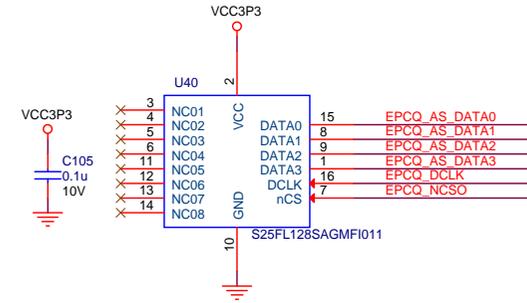
- HEX0[6..0] 4,19
- HEX1[6..0] 4,19
- HEX3[6..0] 4,19



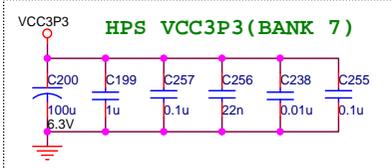
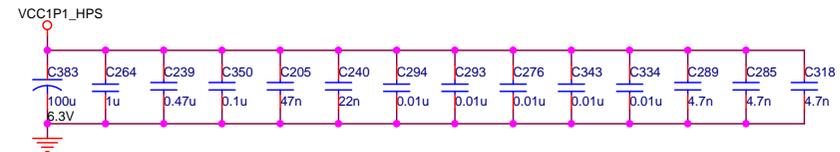
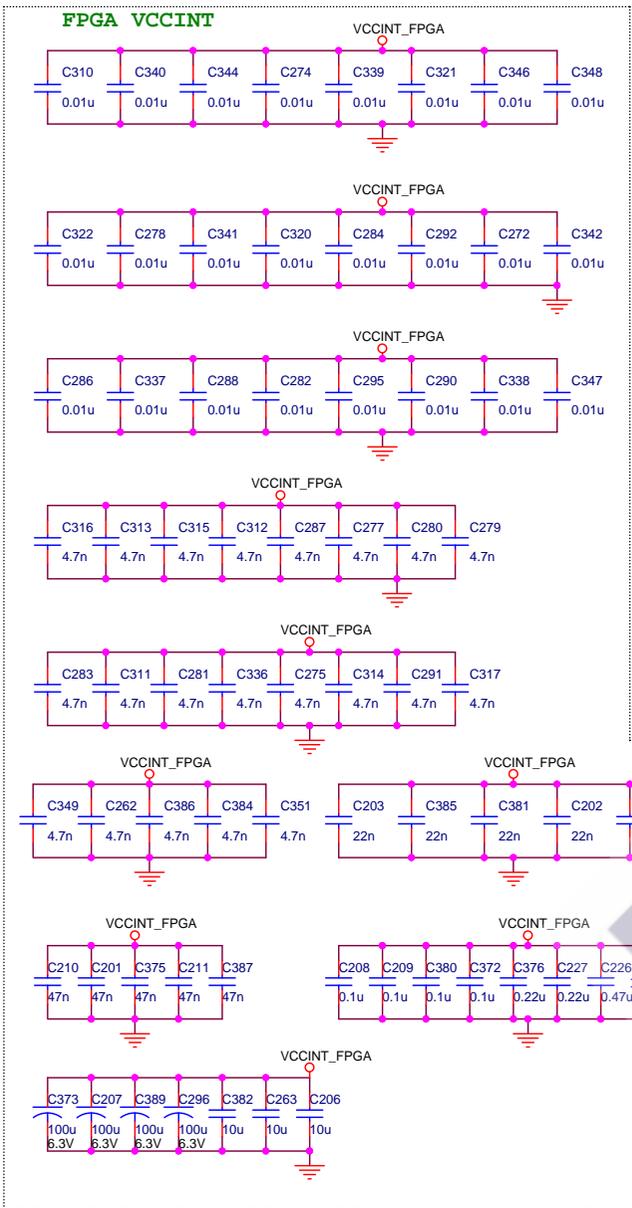
Fix MSEL[4:0]=10010 in AS Fast Mode



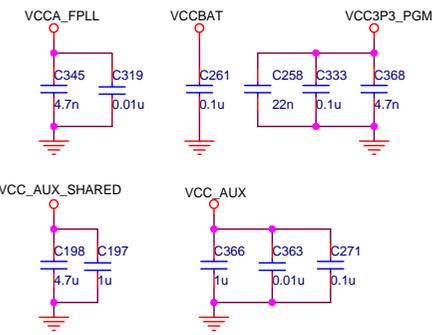
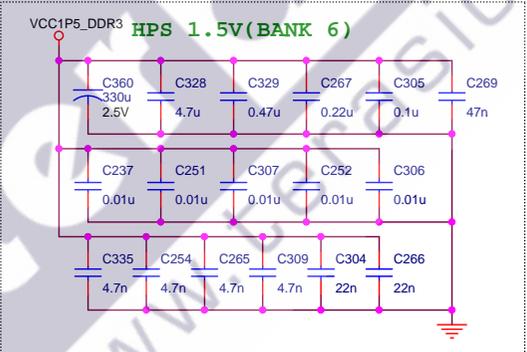
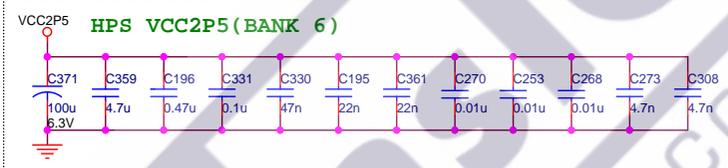
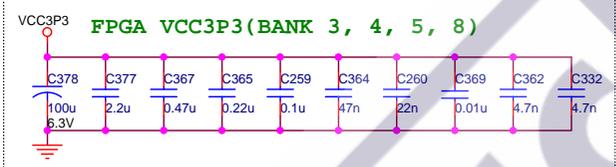
- R138 0 DNI MSEL0
- R137 0 DNI MSEL1
- R125 0 DNI MSEL2
- R124 0 DNI MSEL3
- R123 0 DNI MSEL4



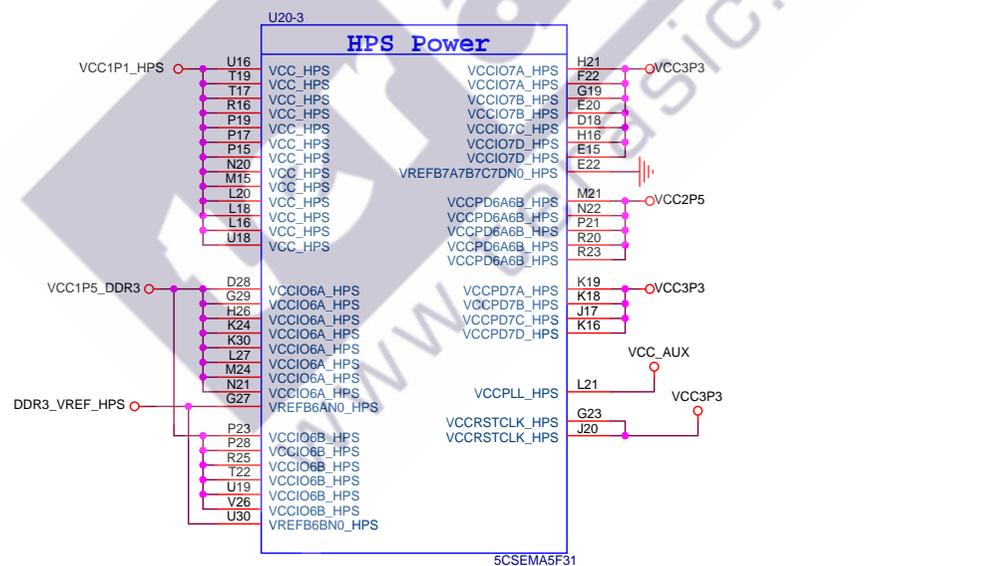
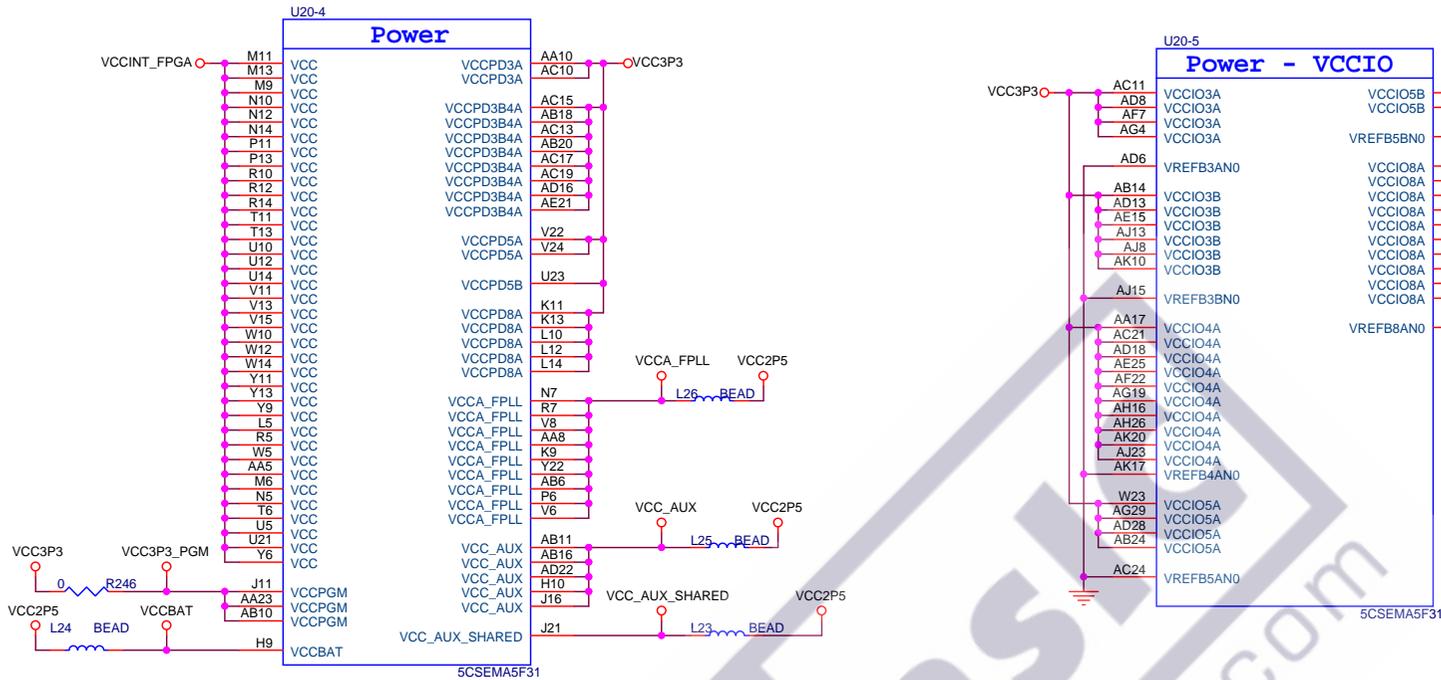
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| Size | Document Number FPGA Configuration | Rev E |
| Date: | Monday, October 20, 2014 | Sheet 7 of 30 |



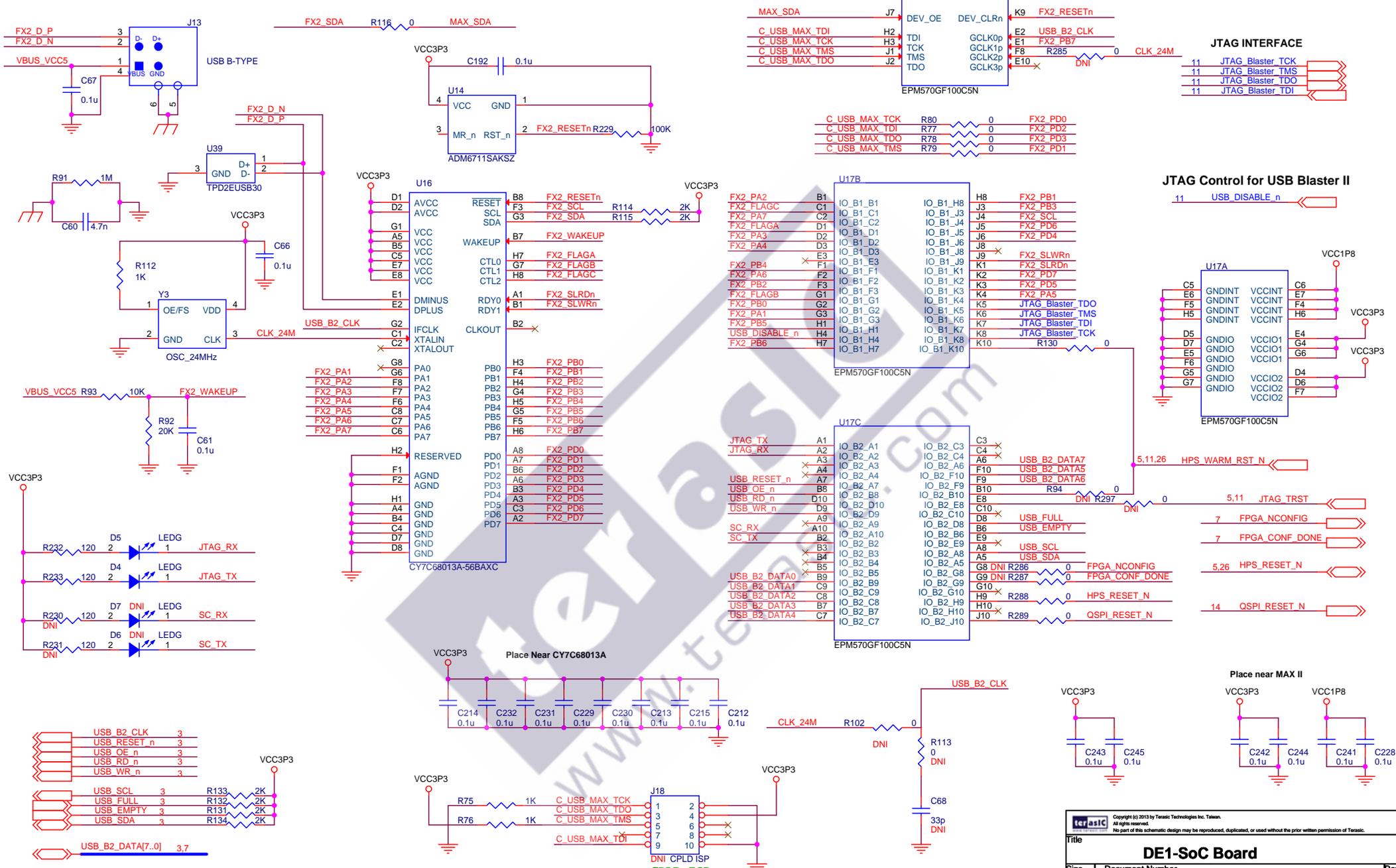
Place C394 close to J20/G23 pin



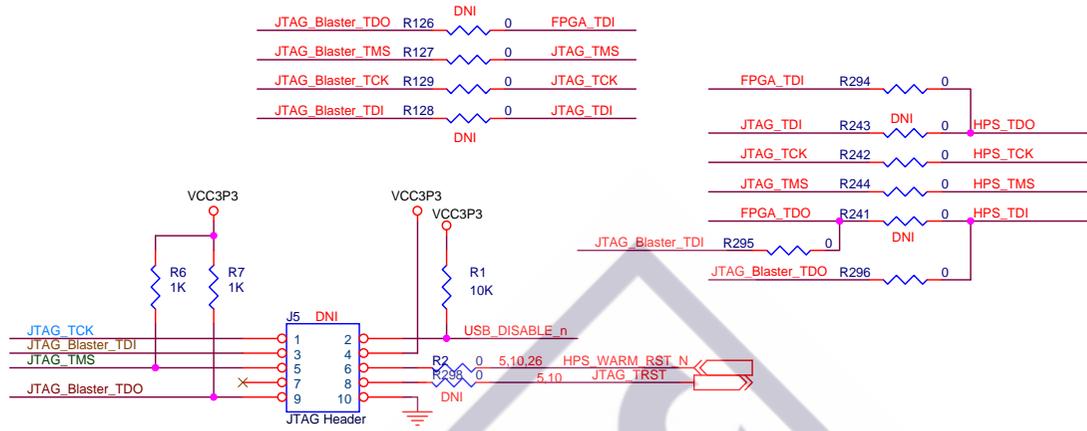
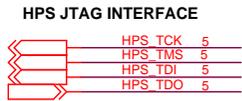
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| FPGA Decoupling | | |
| Date: | Monday, October 20, 2014 | Sheet 8 of 30 |



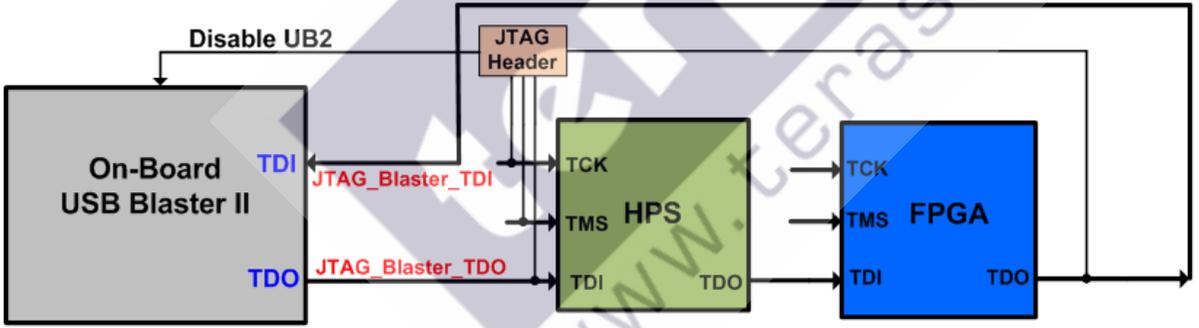
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| DE1-SoC Board | | |
| Size | Document Number | Rev |
| B | FPGA Power | E |
| Date: | Monday, October 20, 2014 | Sheet 9 of 30 |

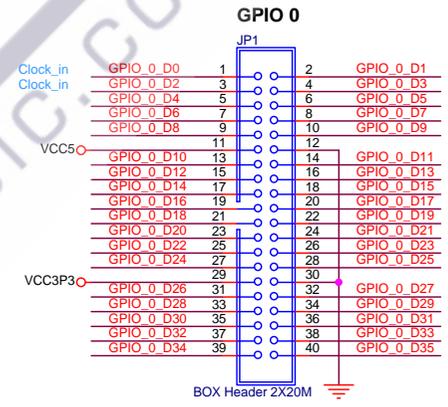
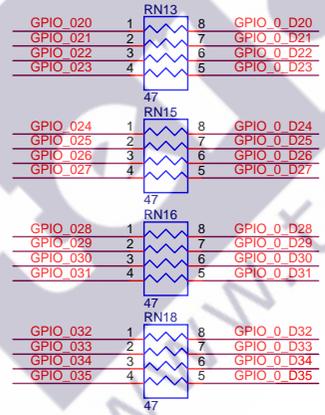
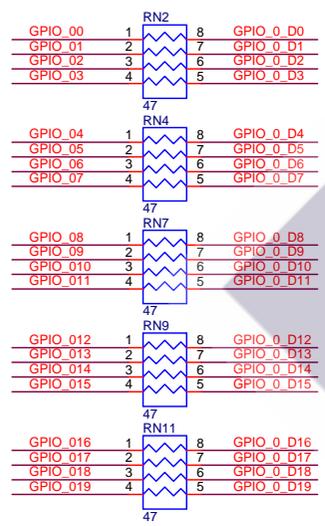
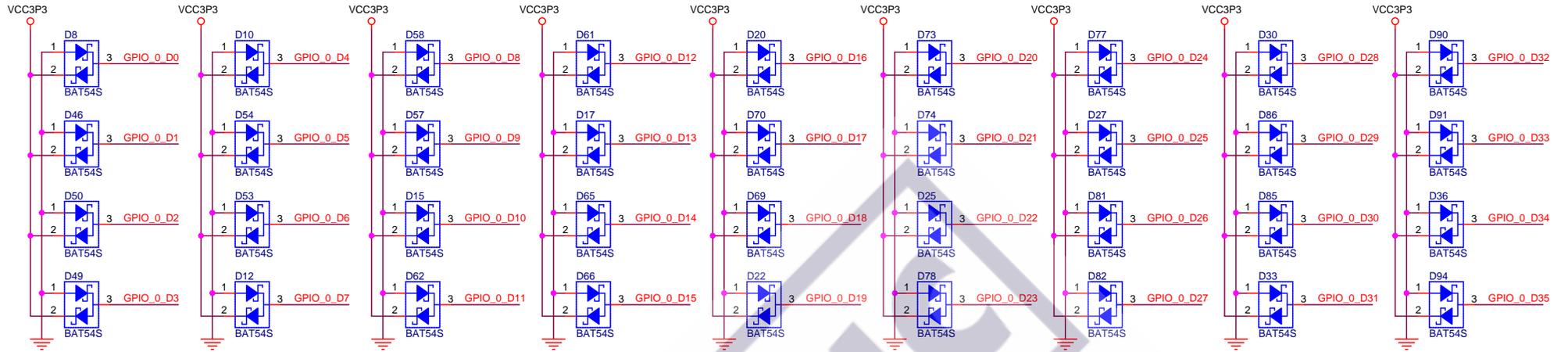


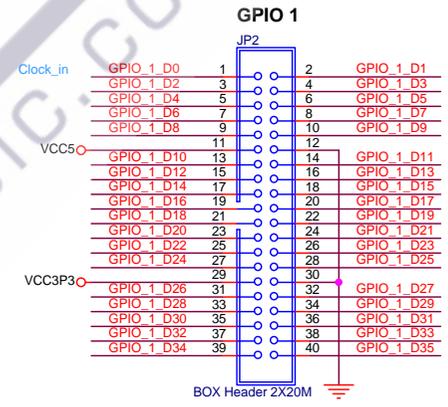
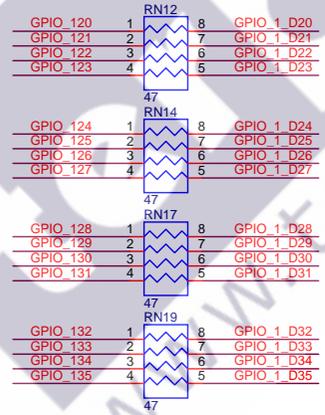
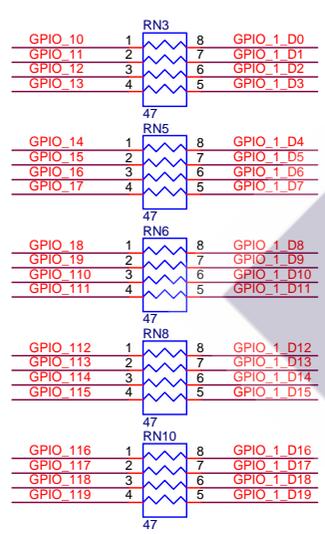
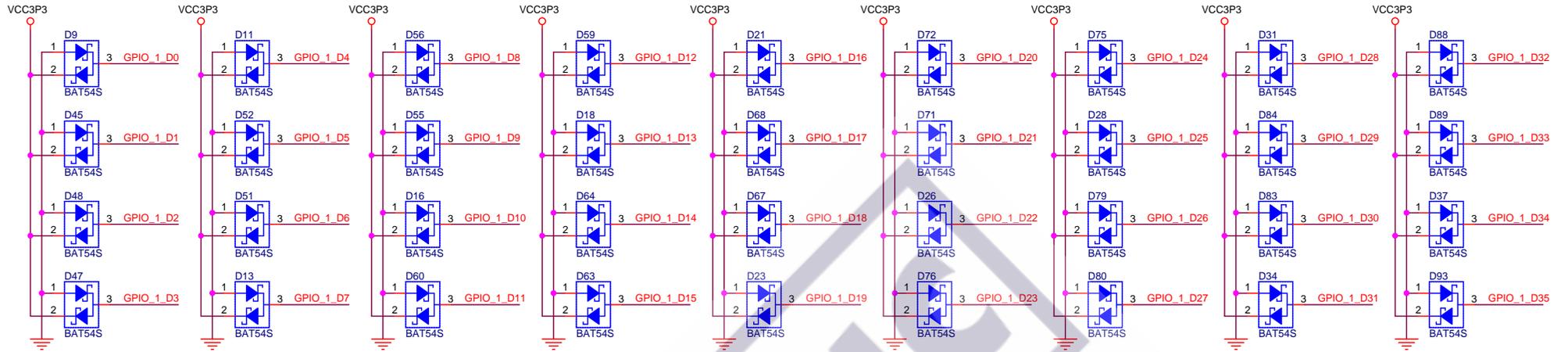
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| Size B | Document Number USB Blaster II | Rev E |
| Date: Monday, October 20, 2014 | Sheet 10 | of 30 |



JTAG Chain







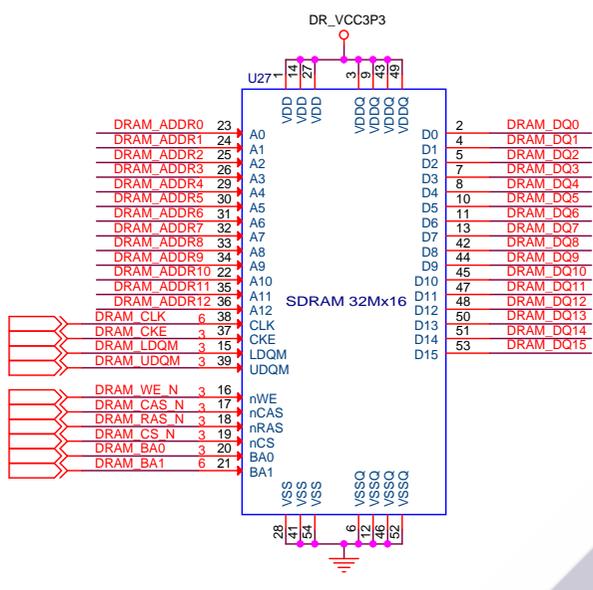
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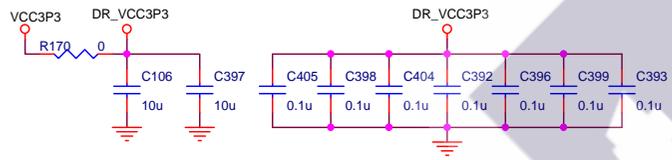
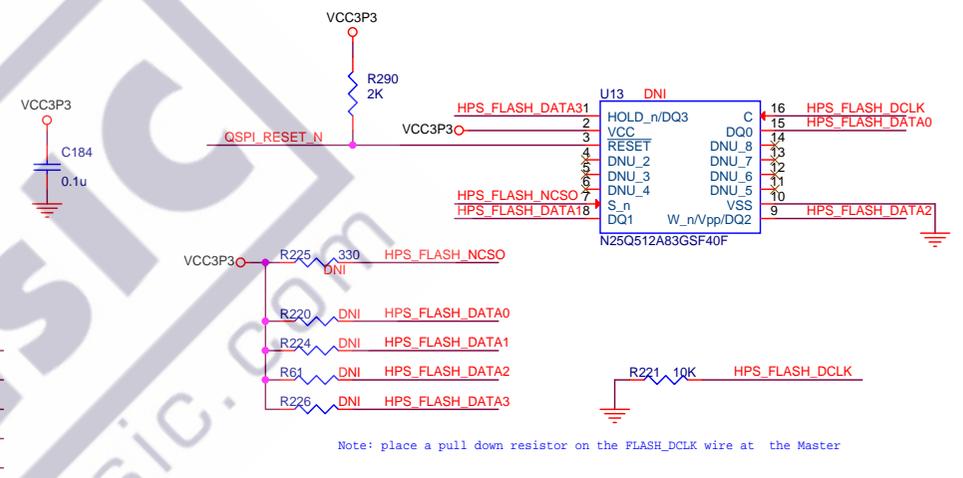
Size B Document Number: **GPIO 1** Rev E

Date: **Monday, October 20, 2014** Sheet **13** of **30**

 DRAM_DQ[15..0] 3
 DRAM_ADDR[12..0] 3,6



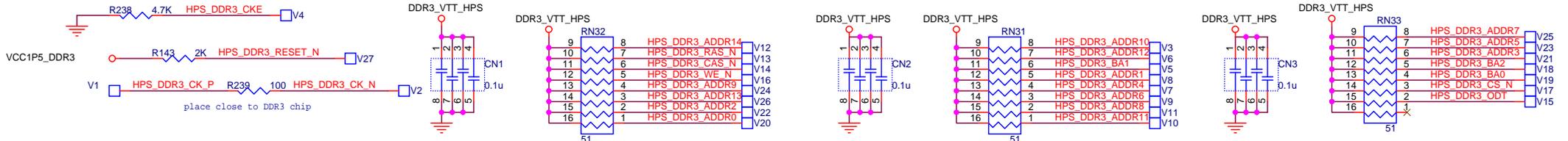
 QSPI_RESET_N 10
 HPS_FLASH_DCLK 5
 HPS_FLASH_DATA[3..0] 5



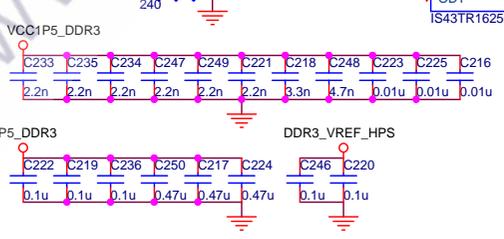
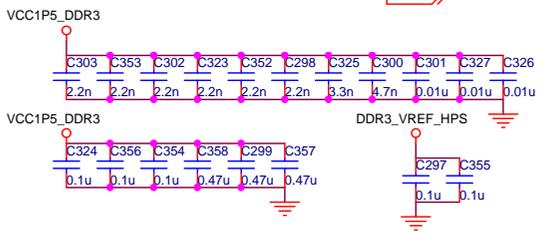
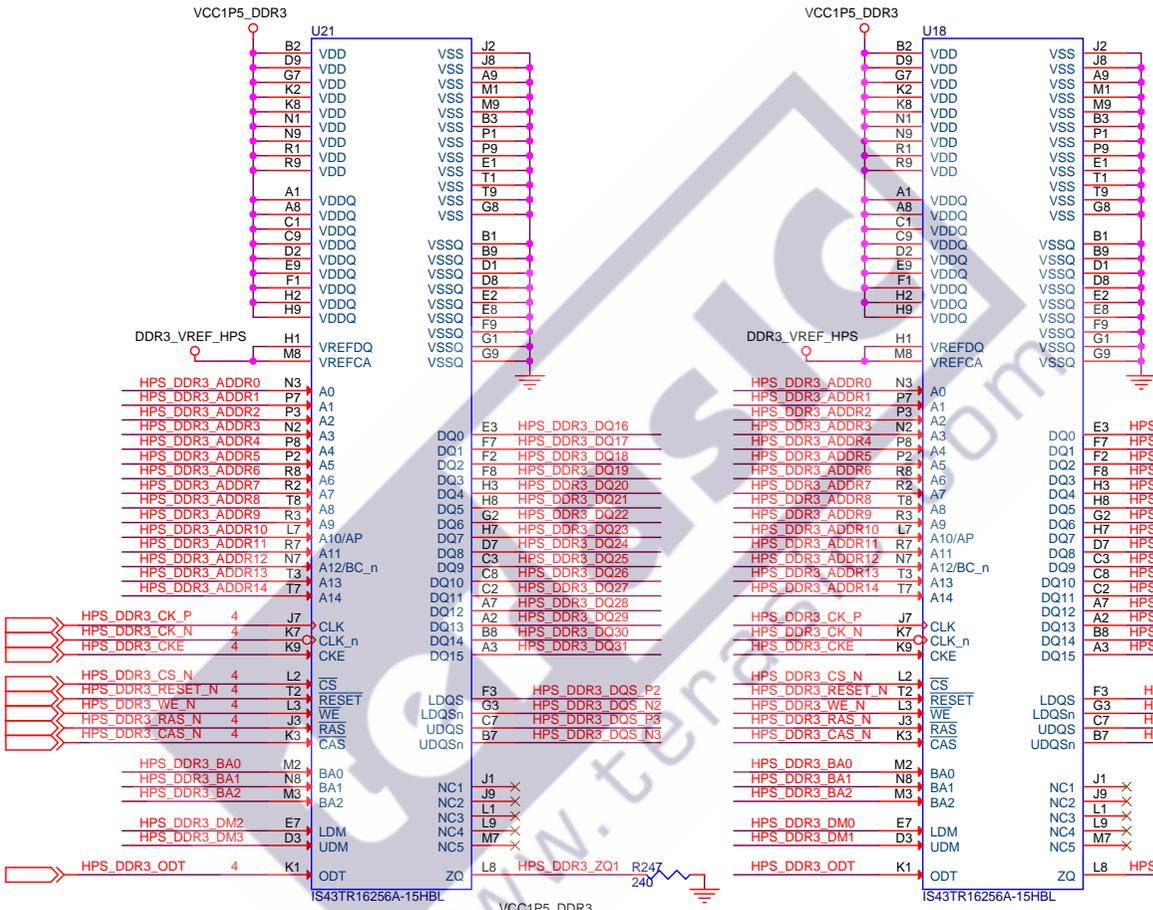
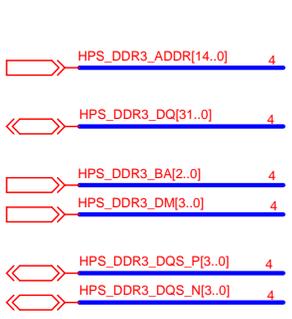
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Title
DE1-SoC Board

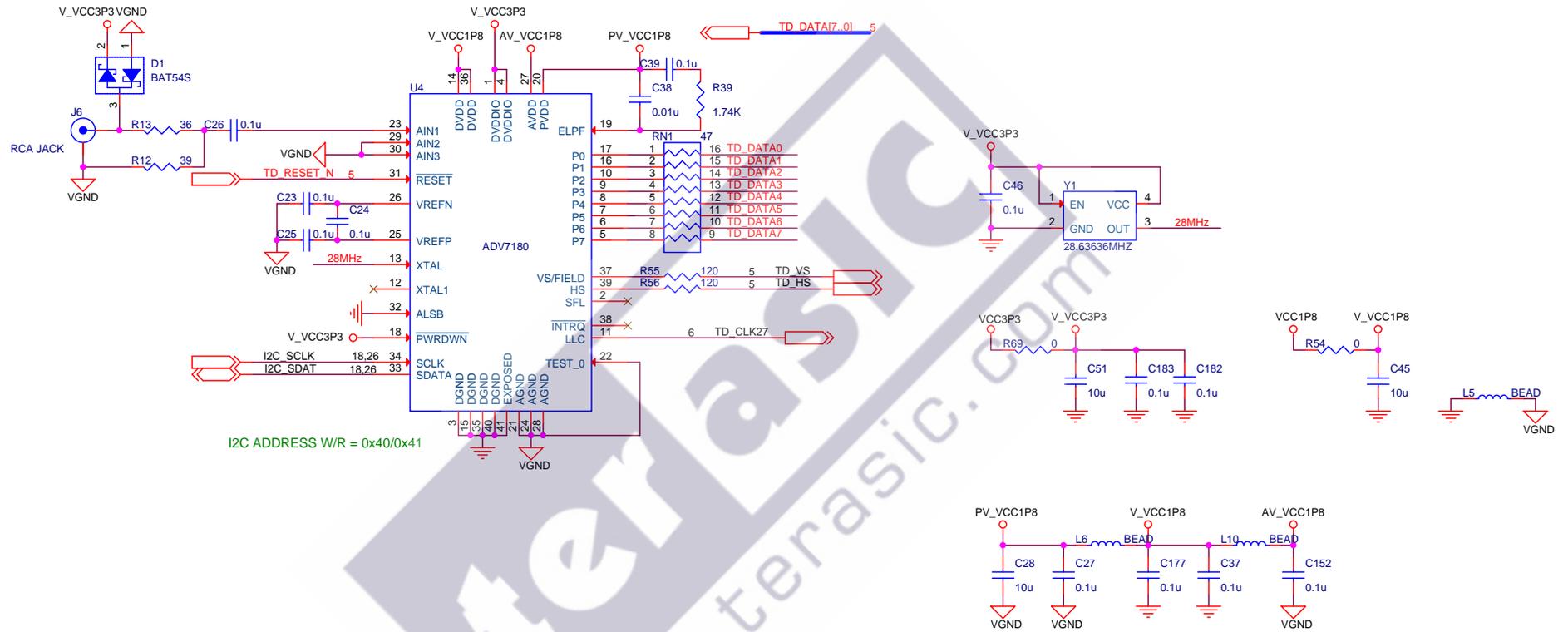
| | | |
|---------------|---|------------------------------|
| Size B | Document Number SDRAM & HPS QSPI Flash | Rev E |
| Date: | Monday, October 20, 2014 | Sheet 14 of 30 |

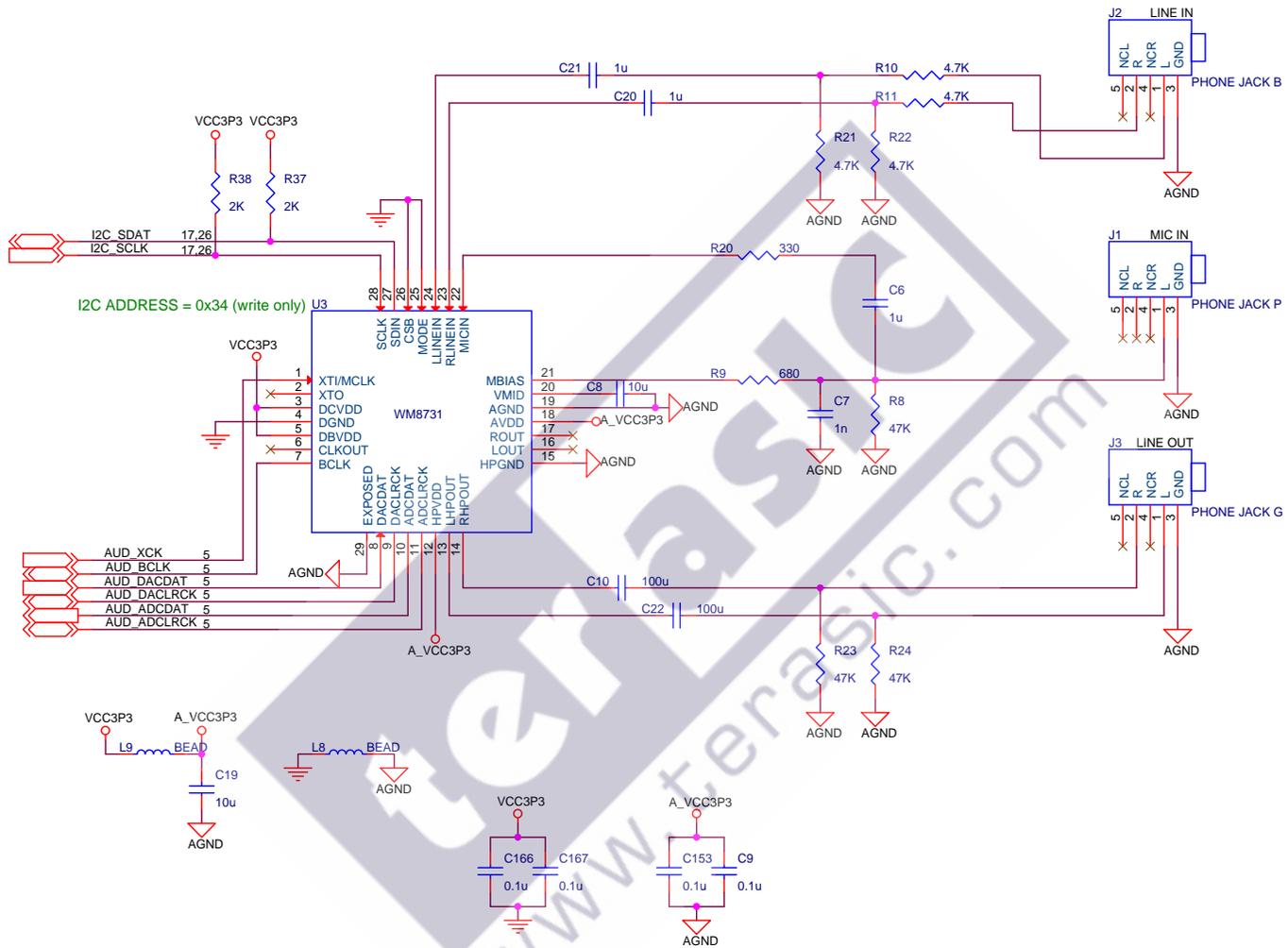


Note: you can only swap the DQ signals within x8 group (e.g. 0-7,8-15,16-23,24-31) on the DDR3 chips Note: you can swap the signals on the OCT resistor array(include NC pin)

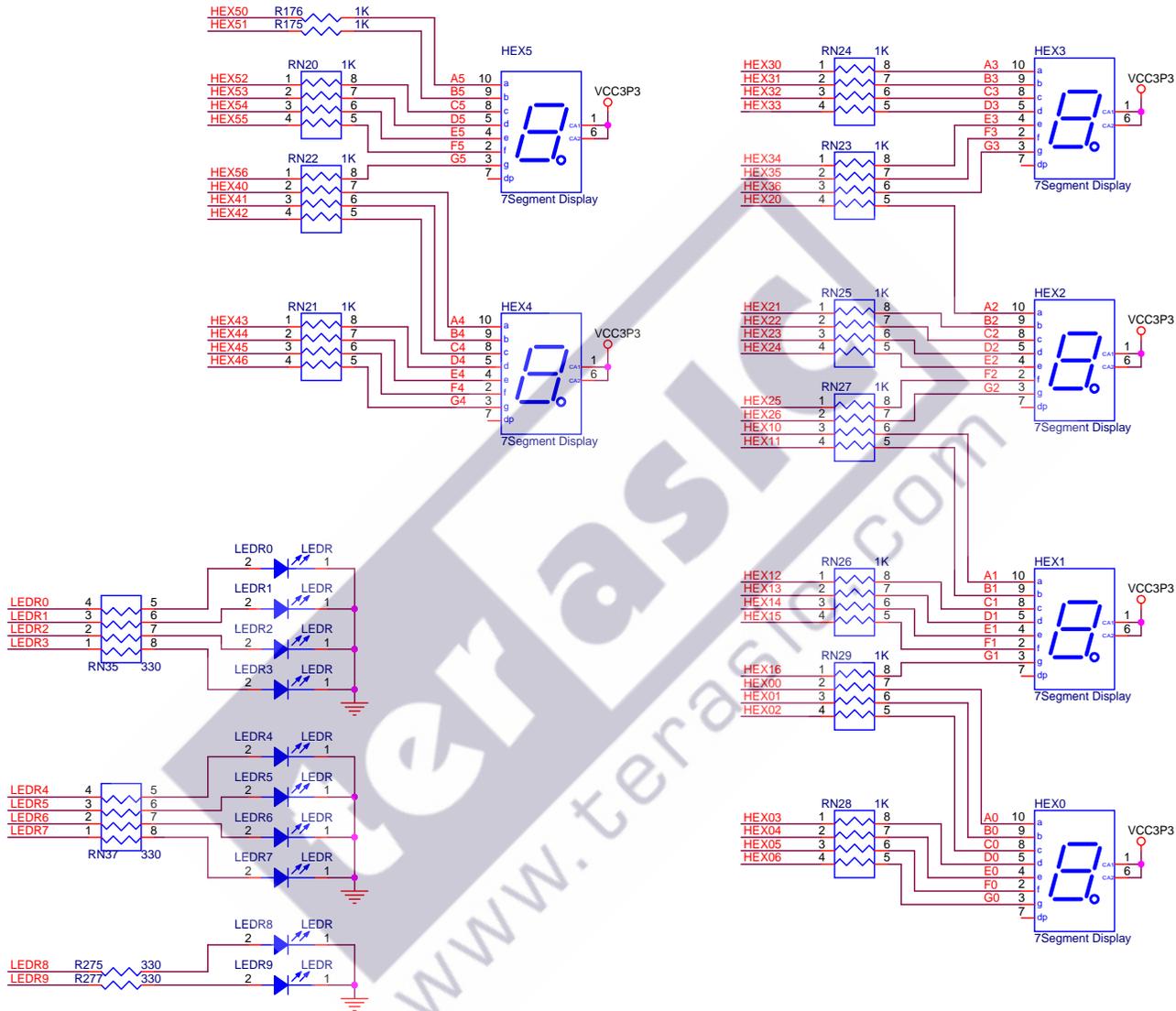
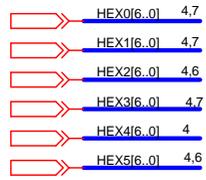


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| Title | | |
| DE1-SoC Board | | |
| Size | Document Number | Rev |
| B | HPS DDR3 SDRAM | E |
| Date: | Monday, October 20, 2014 | Sheet 15 of 30 |



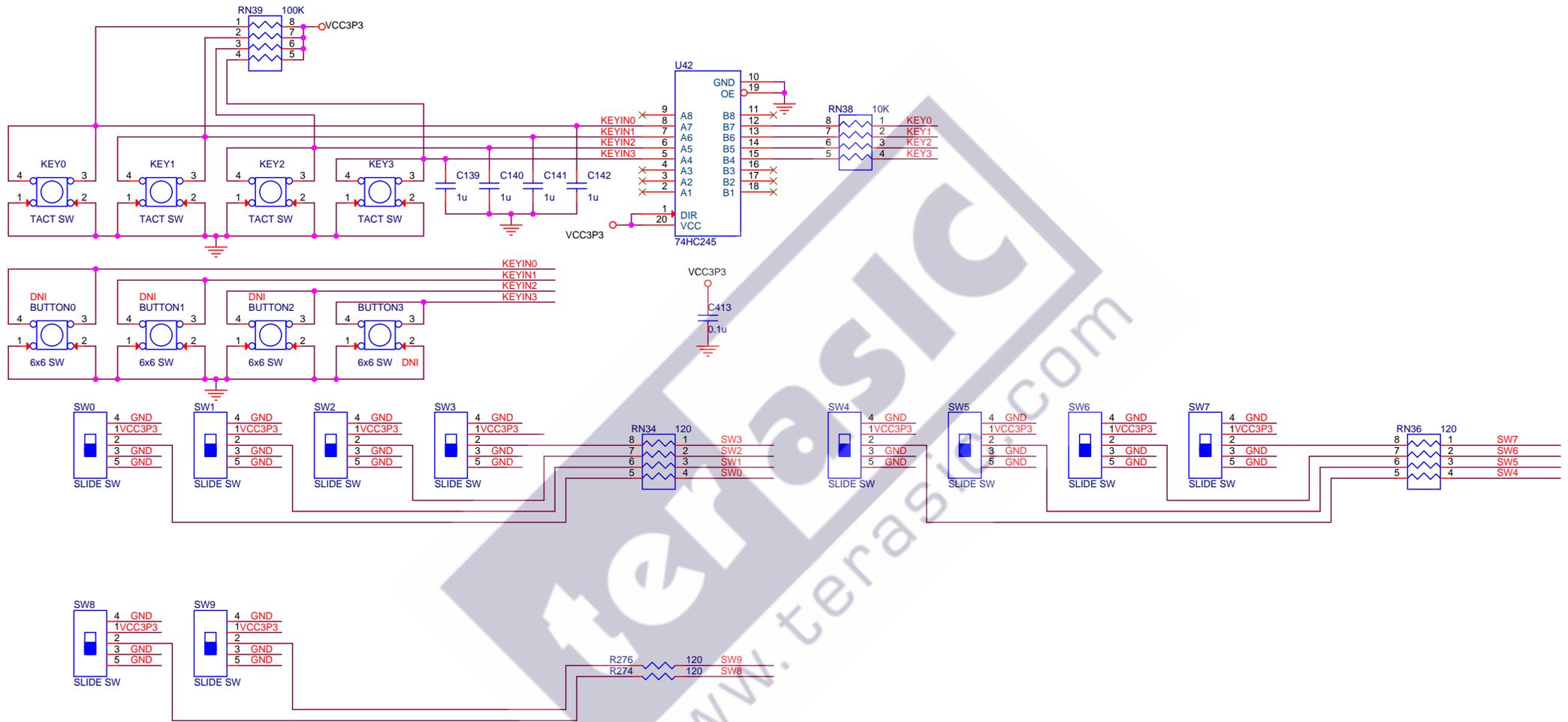


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| Title | |
| DE1-SoC Board | |
| Size | Document Number |
| B | Audio CODEC |
| Date: | Monday, October 20, 2014 |
| Sheet | 18 of 30 |
| Rev | E |

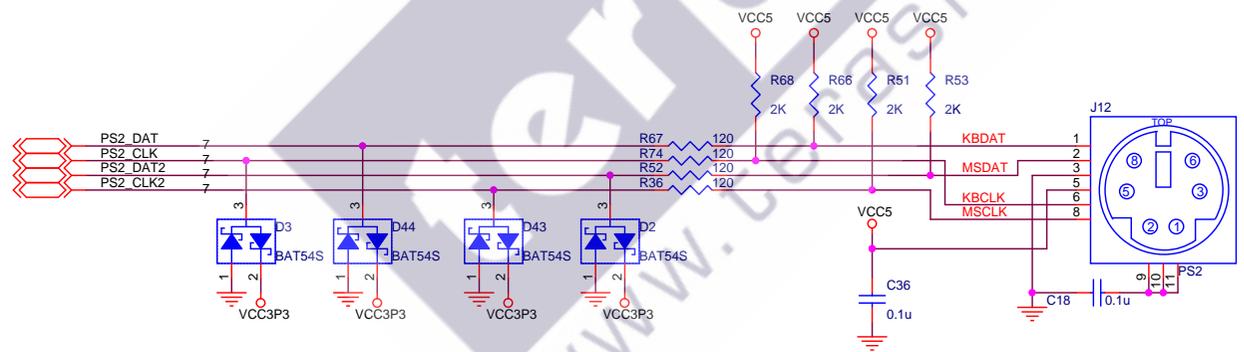
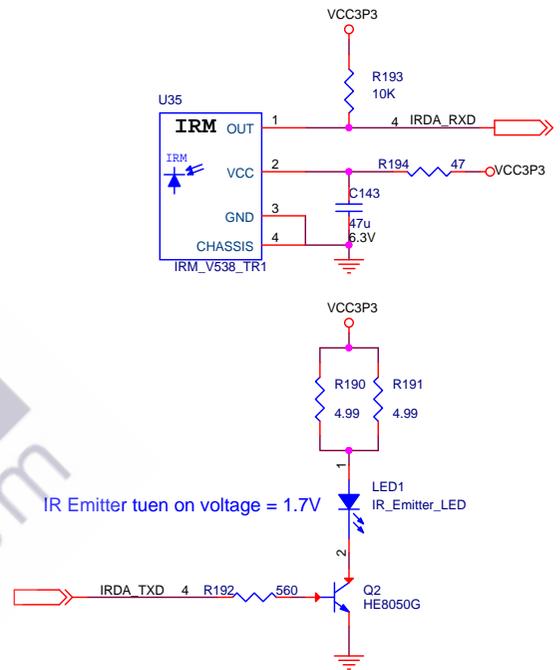
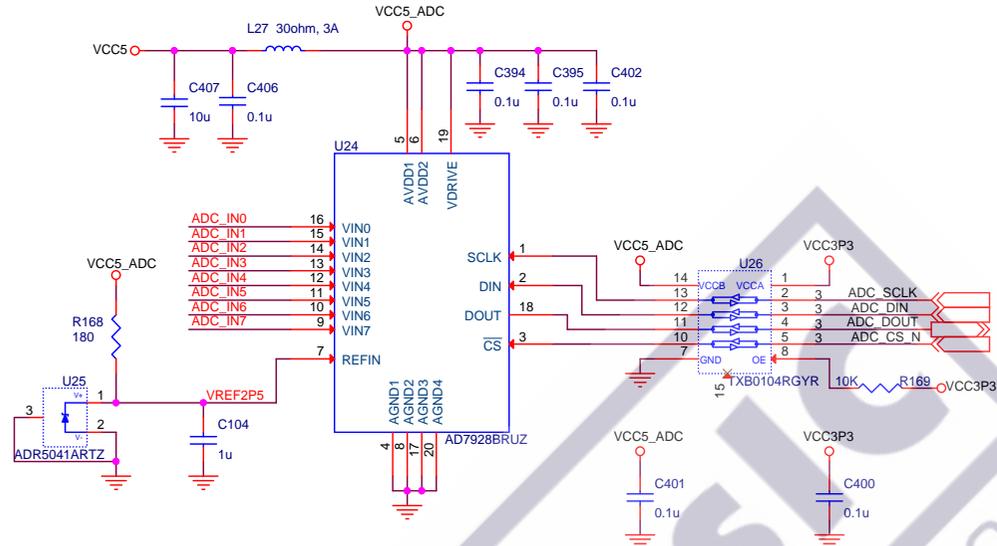
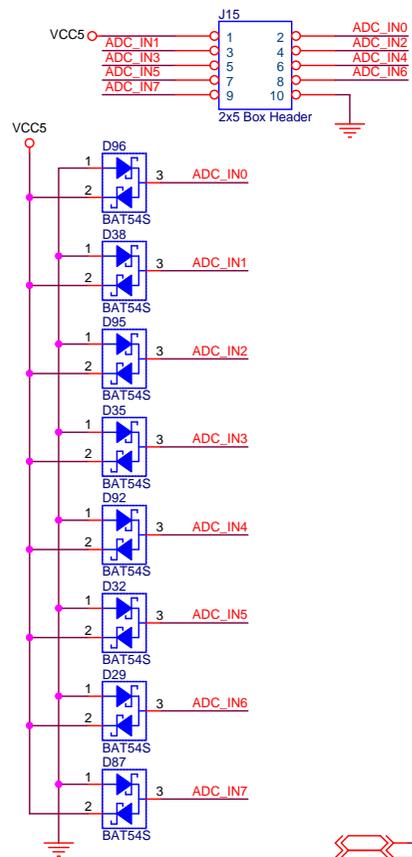


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| Title DE1-SoC Board | | |
| Size B | Document Number 7-Segment Display, LED | Rev E |
| Date: Monday, October 20, 2014 | Sheet 19 | of 30 |

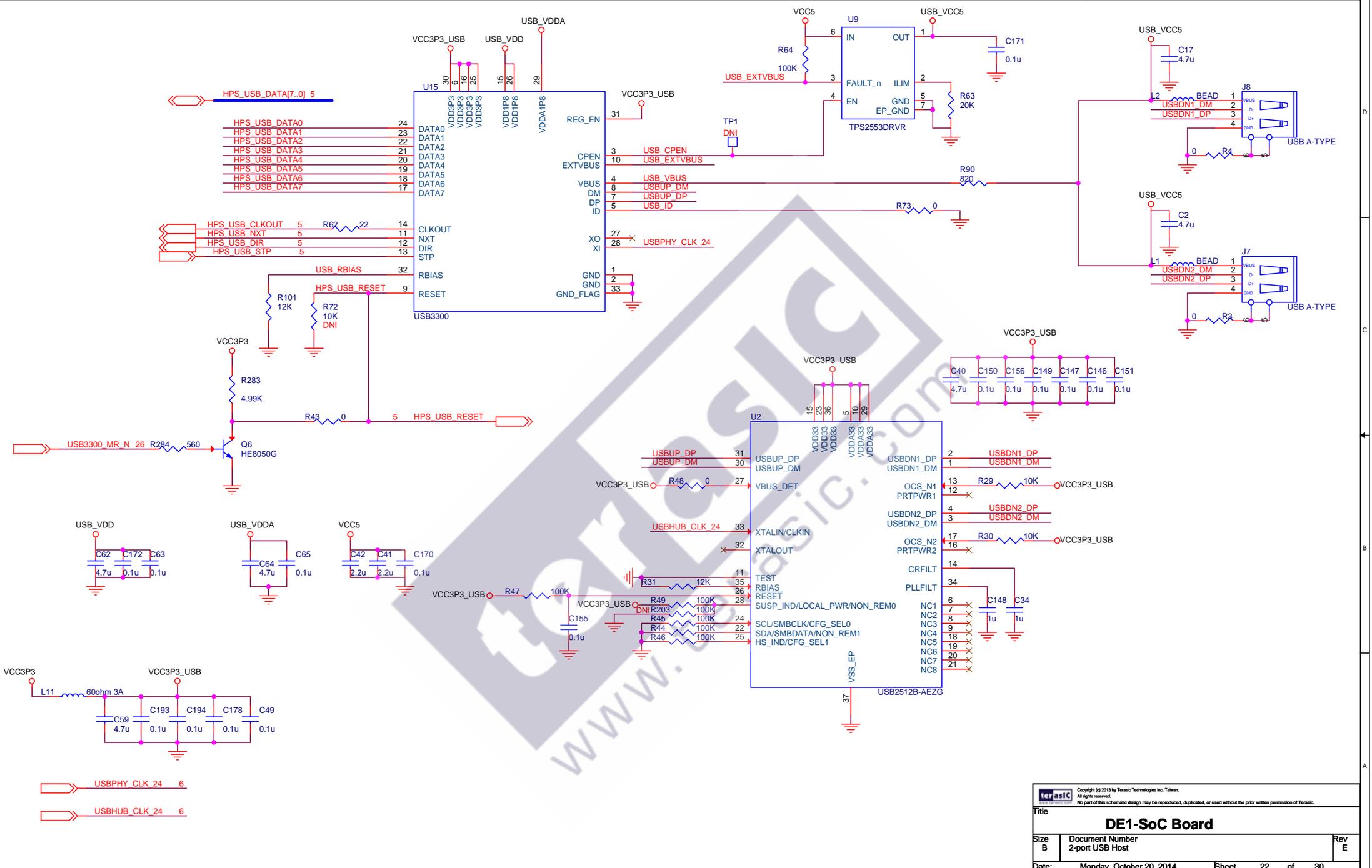
KEY[3..0] 3.6
 SW[9..0] 3.7



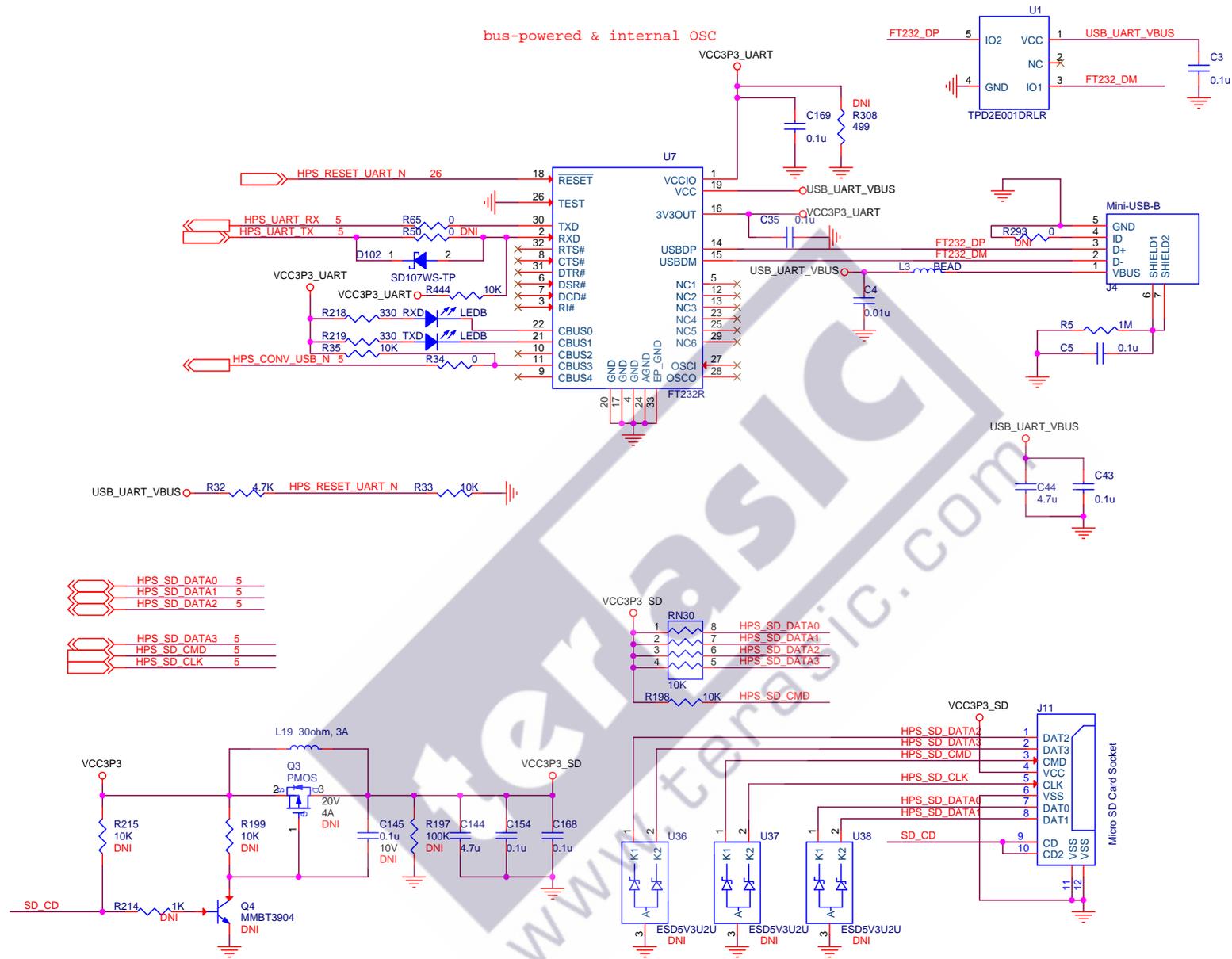
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| Title | | |
| DE1-SoC Board | | |
| Size | Document Number | Rev |
| B | FPGA BUTTON, Switch | E |
| Date: | Monday, October 20, 2014 | Sheet 20 of 30 |



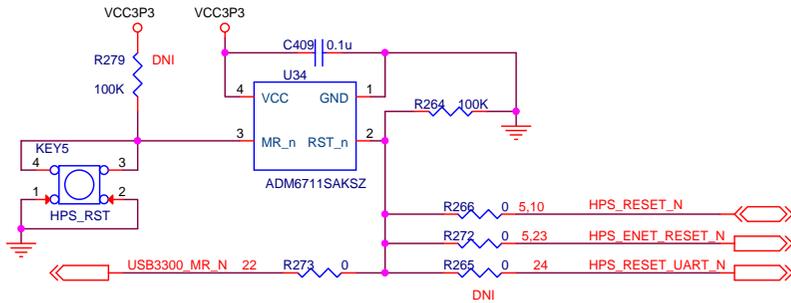
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| Title | | |
| DE1-SoC Board | | |
| Size | Document Number | Rev |
| B | ADC, PS2, IR Tx, IR Rx | E |
| Date: | Monday, October 20, 2014 | Sheet 21 of 30 |



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| Title | | |
| DE1-SoC Board | | |
| Size | Document Number | Rev |
| B | 2-port USB Host | E |
| Date: | Monday, October 20, 2014 | Sheet 22 of 30 |

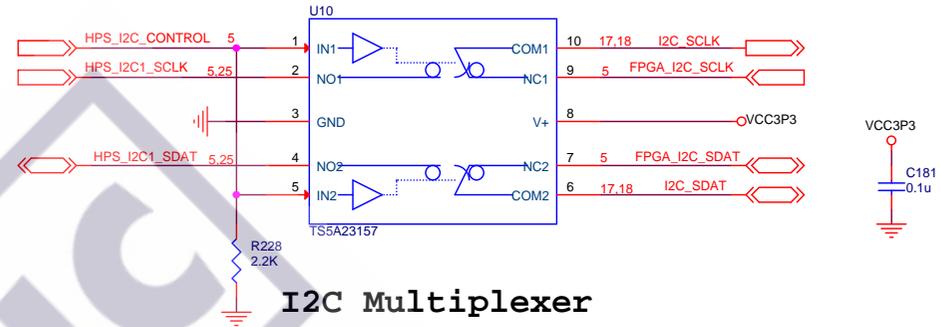


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| Title | | |
| DE1-SoC Board | | |
| Size | Document Number | Rev |
| B | UART to USB, SD CARD | E |
| Date: | Wednesday, October 22, 2014 | Sheet 24 of 30 |

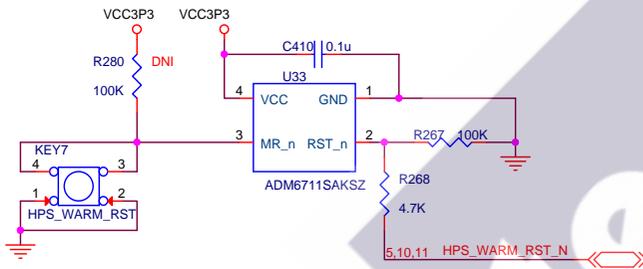


HPS Cold Reset

LOW --> NC to/from COM = ON and NO to/from COM = OFF
 HIGH --> NC to/from COM = OFF and NO to/from COM = ON



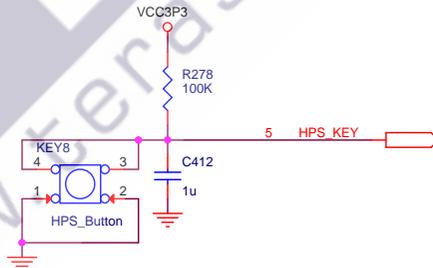
I2C Multiplexer



HPS Warm Reset

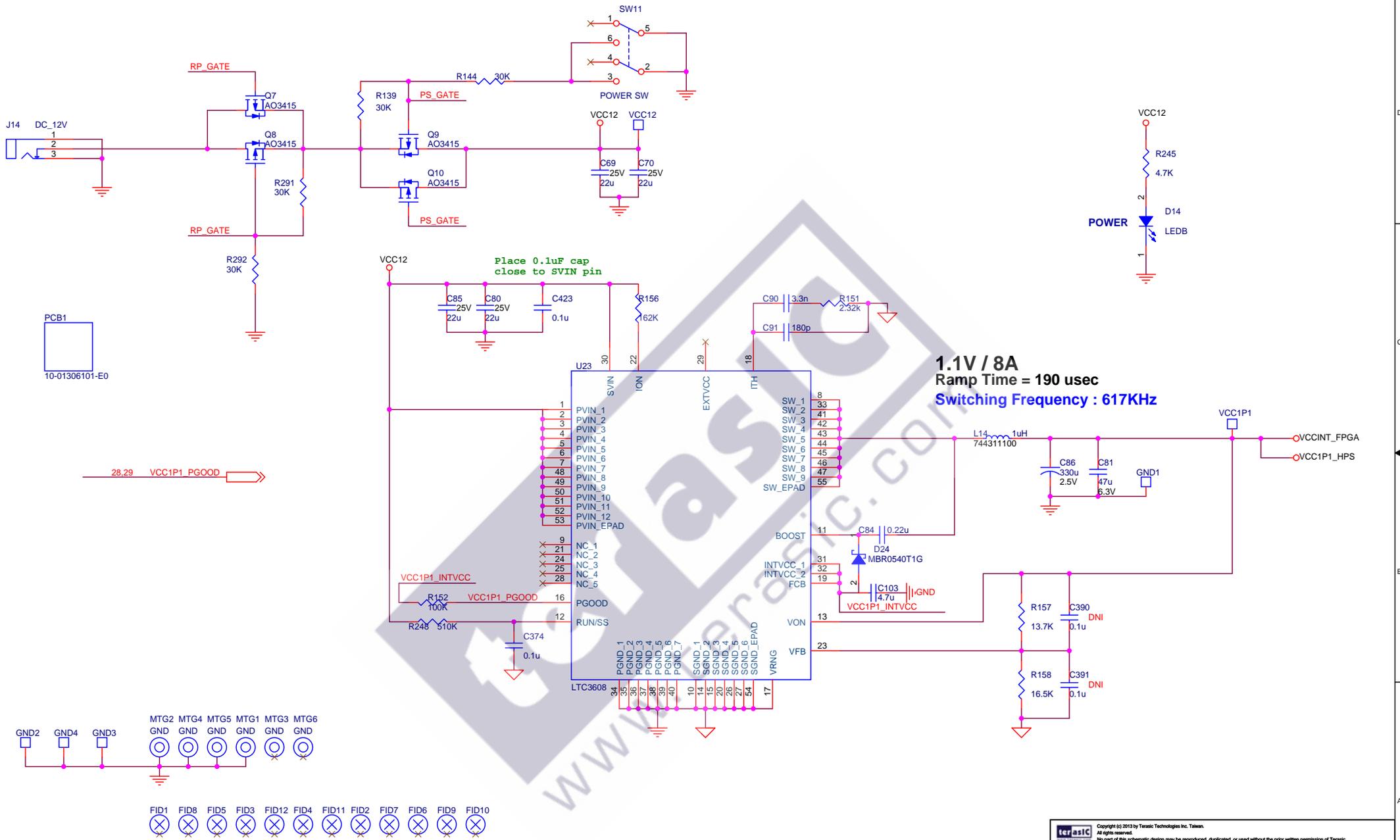


HPS User LED



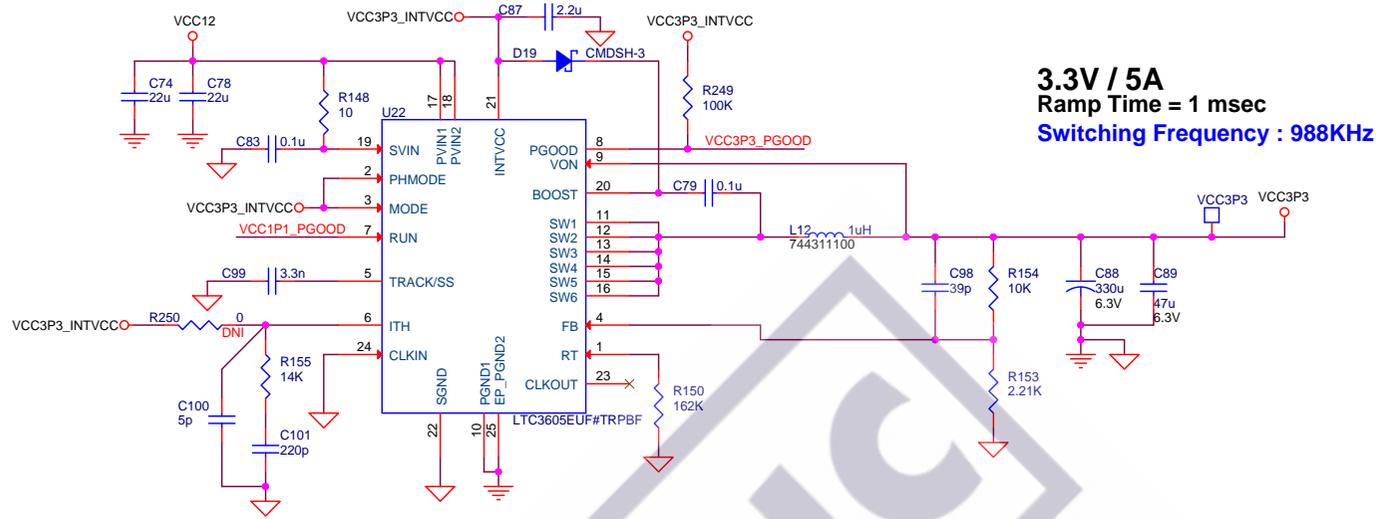
HPS User Button

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| Title | | |
| DE1-SoC Board | | |
| Size | Document Number | Rev |
| B | I2C Multiplexer, HPS BUTTON, HPS LED | E |
| Date: | Monday, October 20, 2014 | Sheet 26 of 30 |

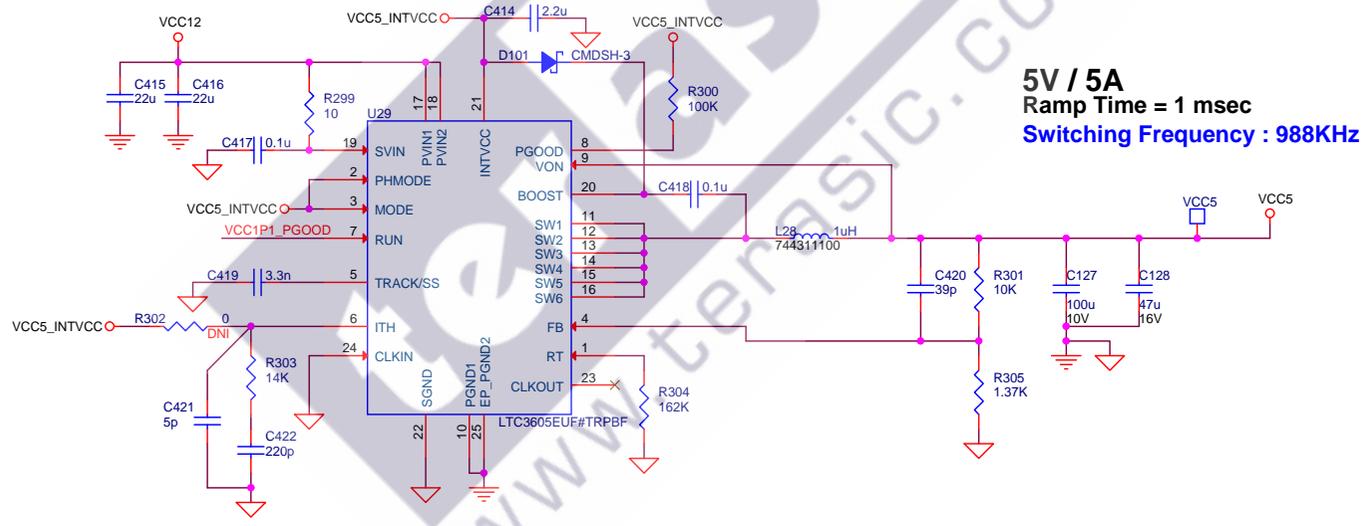


1.1V / 8A
Ramp Time = 190 usec
Switching Frequency : 617KHz

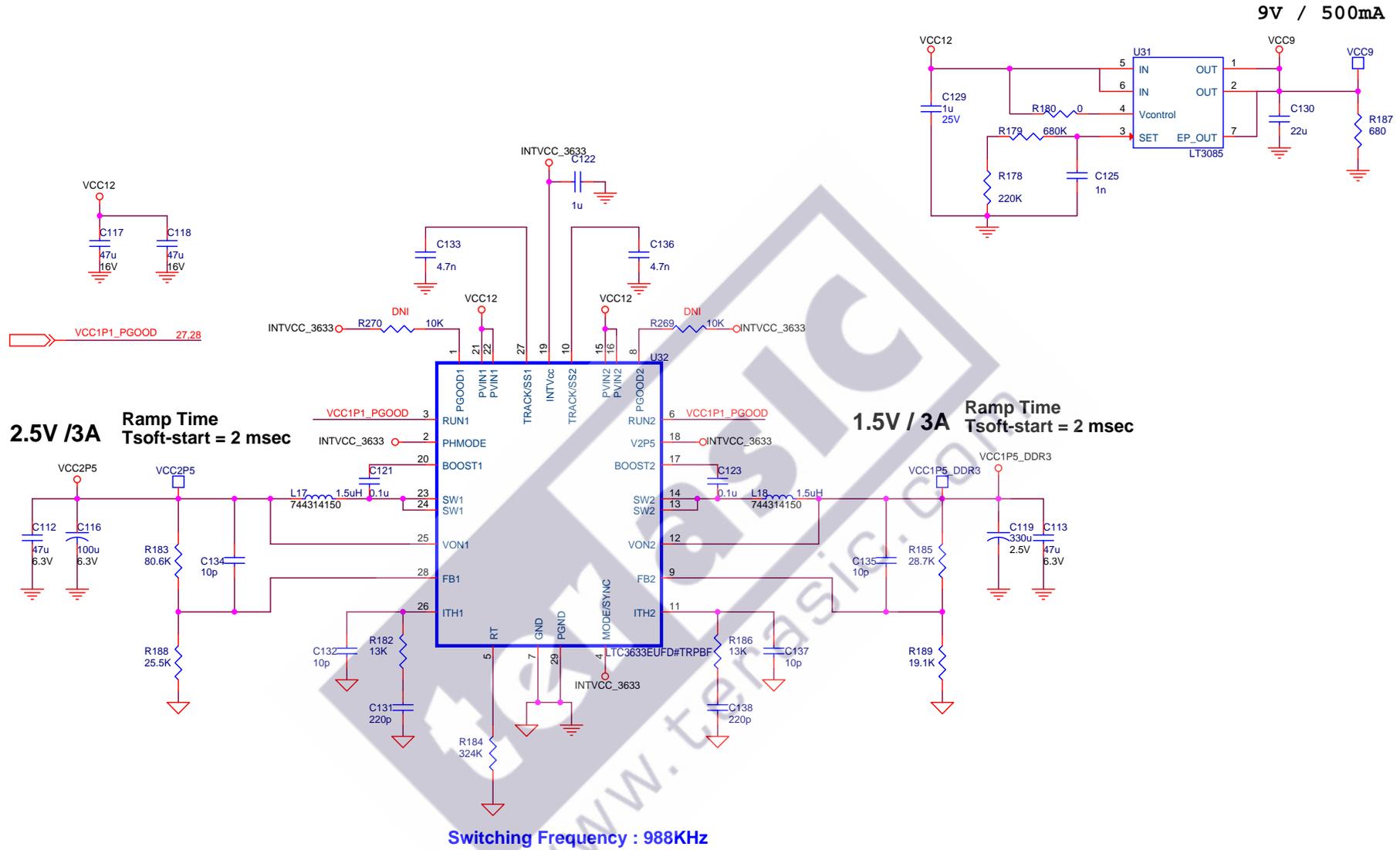
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| Title | | |
| DE1-SoC Board | | |
| Size B | Document Number | Rev E |
| | Power - 1.1V | |
| Date: | Monday, October 20, 2014 | Sheet 27 of 30 |



VCC1P1_PGOOD 27,29



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| Title | | |
| DE1-SoC Board | | |
| Size | Document Number | Rev |
| B | Power - 5V, 3.3V | E |
| Date: | Monday, October 20, 2014 | Sheet 28 of 30 |



2.5V / 3A
Ramp Time
Tsoft-start = 2 msec

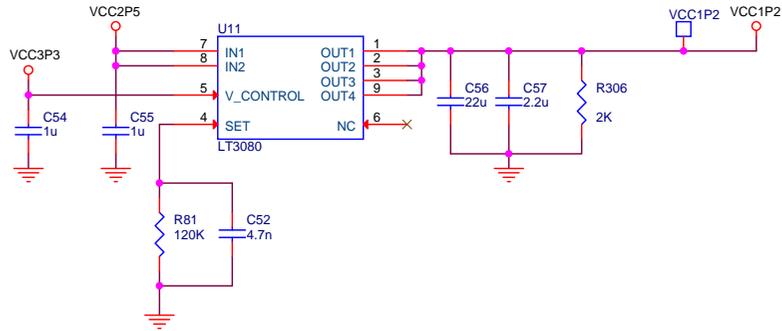
1.5V / 3A
Ramp Time
Tsoft-start = 2 msec

Switching Frequency : 988KHz

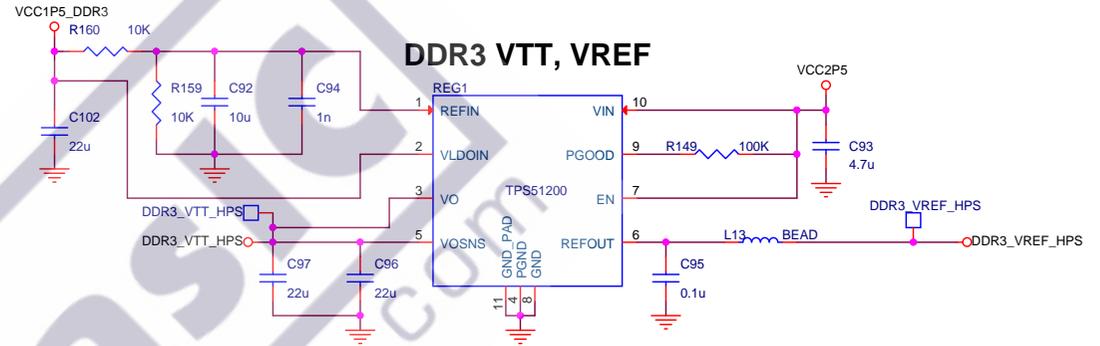
9V / 500mA

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| Title | | |
| DE1-SoC Board | | |
| Size | Document Number | Rev |
| B | Power - 9V, 2.5V, 1.5V | E |
| Date: | Monday, October 20, 2014 | Sheet 29 of 30 |

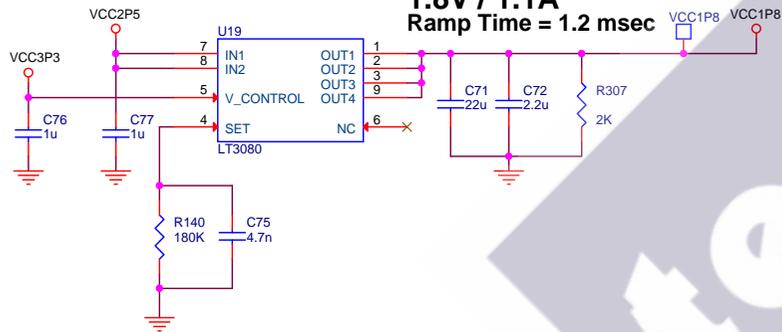
1.2V / 1.1A
Ramp Time = 0.8msec



DDR3 VTT, VREF



1.8V / 1.1A
Ramp Time = 1.2 msec



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| Title | |
| DE1-SoC Board | |
| Size B | Document Number Power - 1.2V, 1.8V, DDR3 VREF, DDR3 VTT |
| Date: | Monday, October 20, 2014 |
| Sheet | 30 of 30 |
| Rev | E |