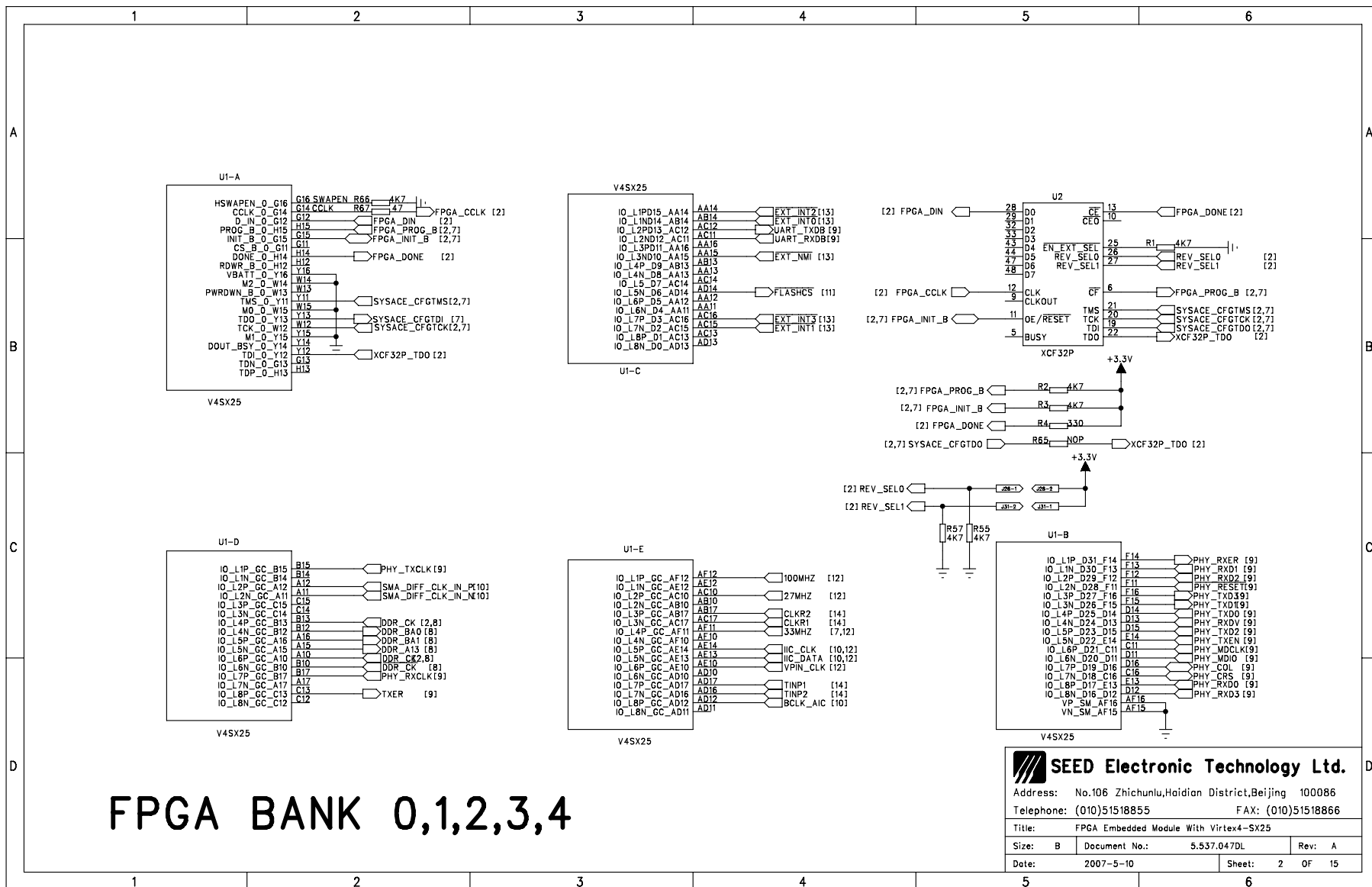
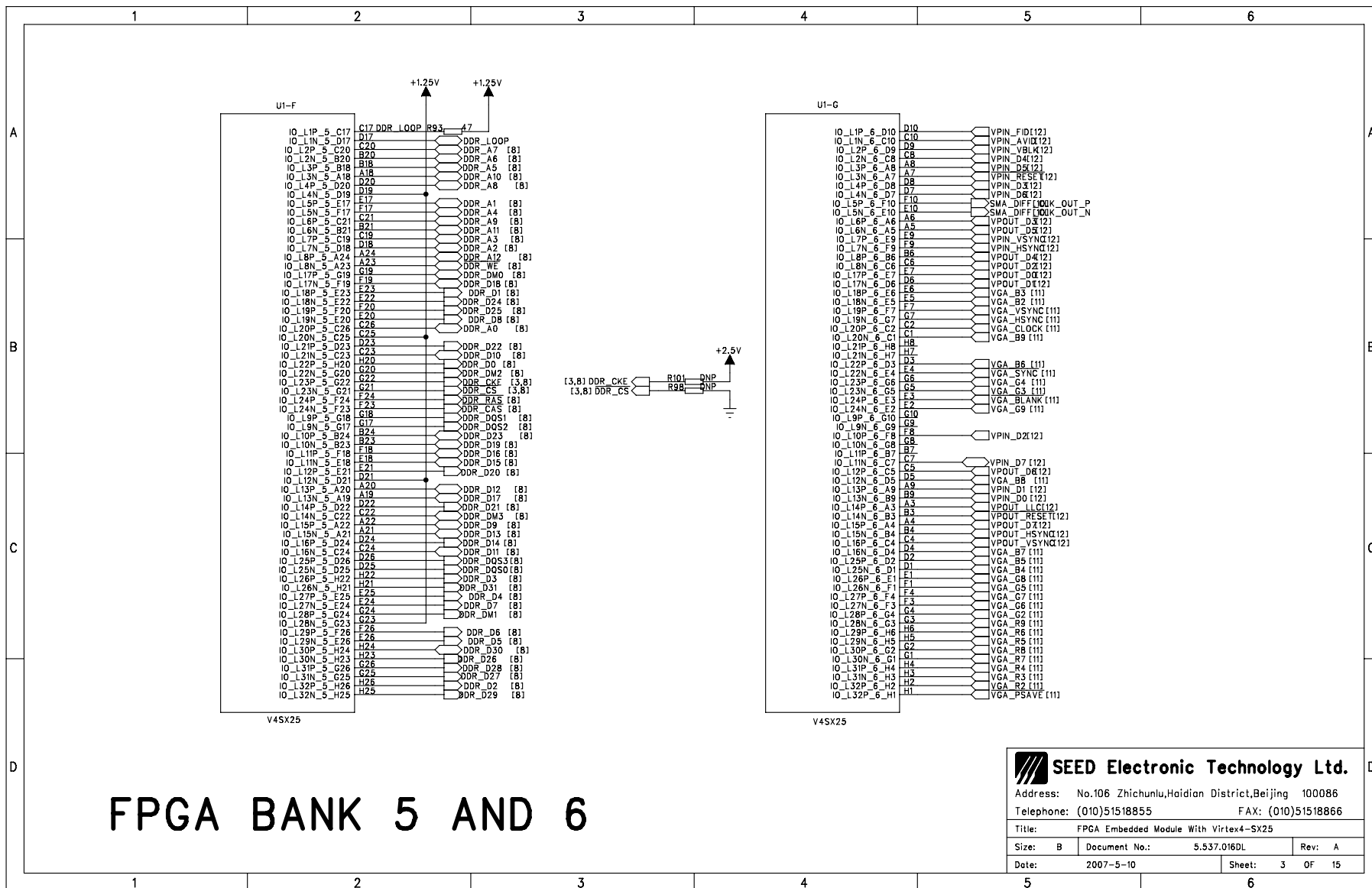


| <p>Notes, Unless Otherwise Specified:</p> <ol style="list-style-type: none"> 1. Resistance Values are in Ohms. 2. Capacitance Values are in Microfarads. 3. Inductance Values are in Microhenries. 4. Highest Reference Designator used: <ul style="list-style-type: none"> A. IC's U44 B. Resistors R203 C. Capacitors C248 D. Inductors L4 E. Transistors Q4 F. LED D1 G. Crystals X4 H. Connectors/Headers J8 I. Switches SW1 J. Test Points TP4 5. The following is the list of uninstalled parts: | | | | <p>Revisions</p> <table border="1" style="width:100%; border-collapse: collapse;"> <thead> <tr> <th style="width:10%;">REV</th> <th style="width:60%;">Description</th> <th style="width:15%;">Date</th> <th style="width:15%;">Approved</th> </tr> </thead> <tbody> <tr> <td>A</td> <td>SEED-FEM025v1.0</td> <td>2007-5-20</td> <td>Mark Qian</td> </tr> <tr> <td>B</td> <td>SEED-FEM025v2.0</td> <td>2008-6-20</td> <td>Mark Qian</td> </tr> </tbody> </table> | | REV | Description | Date | Approved | A | SEED-FEM025v1.0 | 2007-5-20 | Mark Qian | B | SEED-FEM025v2.0 | 2008-6-20 | Mark Qian | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | | REV | Description | Date | Approved | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | A | SEED-FEM025v1.0 | 2007-5-20 | Mark Qian | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| | | | | B | SEED-FEM025v2.0 | 2008-6-20 | Mark Qian | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| | | | | <p>Sheet:</p> <hr/> <table style="width:100%;"> <tr> <td style="width:50%;">1. Cover Sheet</td> <td style="width:50%;">15. POWER OUTPUT</td> </tr> <tr> <td>2. FPGA BANK 0,1,2,3,4</td> <td></td> </tr> <tr> <td>3. FPGA BANK 5 AND 6</td> <td></td> </tr> <tr> <td>4. FPGA BANK 7 AND 8</td> <td></td> </tr> <tr> <td>5. RESERVE PIN</td> <td></td> </tr> <tr> <td>6. FPGA POWER</td> <td></td> </tr> <tr> <td>7. SYSACE & CF</td> <td></td> </tr> <tr> <td>8. DDR SDRAM</td> <td></td> </tr> <tr> <td>9. UART & ETHERNET</td> <td></td> </tr> <tr> <td>10. AUDIO & DIFF CLK</td> <td></td> </tr> <tr> <td>11. VGA OUTPUT SRAM & FLASH</td> <td></td> </tr> <tr> <td>12. VIDEO IN & VIDEO OUT & CLOCK</td> <td></td> </tr> <tr> <td>13. MEMORY EXTEND BUS</td> <td></td> </tr> <tr> <td>14. EXTEND PERIPHERALS BUS</td> <td></td> </tr> </table> | | 1. Cover Sheet | 15. POWER OUTPUT | 2. FPGA BANK 0,1,2,3,4 | | 3. FPGA BANK 5 AND 6 | | 4. FPGA BANK 7 AND 8 | | 5. RESERVE PIN | | 6. FPGA POWER | | 7. SYSACE & CF | | 8. DDR SDRAM | | 9. UART & ETHERNET | | 10. AUDIO & DIFF CLK | | 11. VGA OUTPUT SRAM & FLASH | | 12. VIDEO IN & VIDEO OUT & CLOCK | | 13. MEMORY EXTEND BUS | | 14. EXTEND PERIPHERALS BUS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| 4. FPGA BANK 7 AND 8 | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 5. RESERVE PIN | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 6. FPGA POWER | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 7. SYSACE & CF | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 8. DDR SDRAM | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 9. UART & ETHERNET | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 10. AUDIO & DIFF CLK | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 11. VGA OUTPUT SRAM & FLASH | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 12. VIDEO IN & VIDEO OUT & CLOCK | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 13. MEMORY EXTEND BUS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| 14. EXTEND PERIPHERALS BUS | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| <table border="1" style="width:100%; border-collapse: collapse;"> <thead> <tr> <th colspan="8">Revision Status of Sheets</th> </tr> <tr> <th>REV</th> <th>1</th> <th>2</th> <th>3</th> <th>4</th> <th>5</th> <th>6</th> <th>7</th> </tr> </thead> <tbody> <tr> <td>SH</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> <tr> <td>REV</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> <tr> <td>SH</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> <tr> <td>REV</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> <tr> <td>SH</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> <tr> <td>REV</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> <tr> <td>SH</td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> </tbody> </table> | | | | Revision Status of Sheets | | | | | | | | REV | 1 | 2 | 3 | 4 | 5 | 6 | 7 | SH | | | | | | | | REV | | | | | | | | SH | | | | | | | | REV | | | | | | | | SH | | | | | | | | REV | | | | | | | | SH | | | | | | | | <table border="1" style="width:100%; border-collapse: collapse;"> <tr> <td>DWN: Dzb</td> <td>Date:2008-06-20</td> </tr> <tr> <td>CHK:</td> <td>Date:</td> </tr> <tr> <td>ENGR:</td> <td>Date:</td> </tr> <tr> <td>MGR:</td> <td>Date:</td> </tr> <tr> <td>QA:</td> <td>Date:</td> </tr> <tr> <td>MFG:</td> <td>Date:</td> </tr> <tr> <td>RLSE:</td> <td>Date:</td> </tr> </table> | | DWN: Dzb | Date:2008-06-20 | CHK: | Date: | ENGR: | Date: | MGR: | Date: | QA: | Date: | MFG: | Date: | RLSE: | Date: |
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| QA: | Date: | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| RLSE: | Date: | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
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| Application | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |

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|---|---------------------------|
| SEED Electronic Technology Ltd. | |
| Address: No.106 Zhichunlu,Haidian District,Beijing 100086 Telephone: (010)51518855 FAX: (010)51518866 | |
| Title: FPGA Embedded Module With Virtex4-SX25 | |
| Size: B | Document No.: 5.537.047DL |
| Date: 2008-6-20 | Rev: B |
| Sheet: 1 | OF 15 |

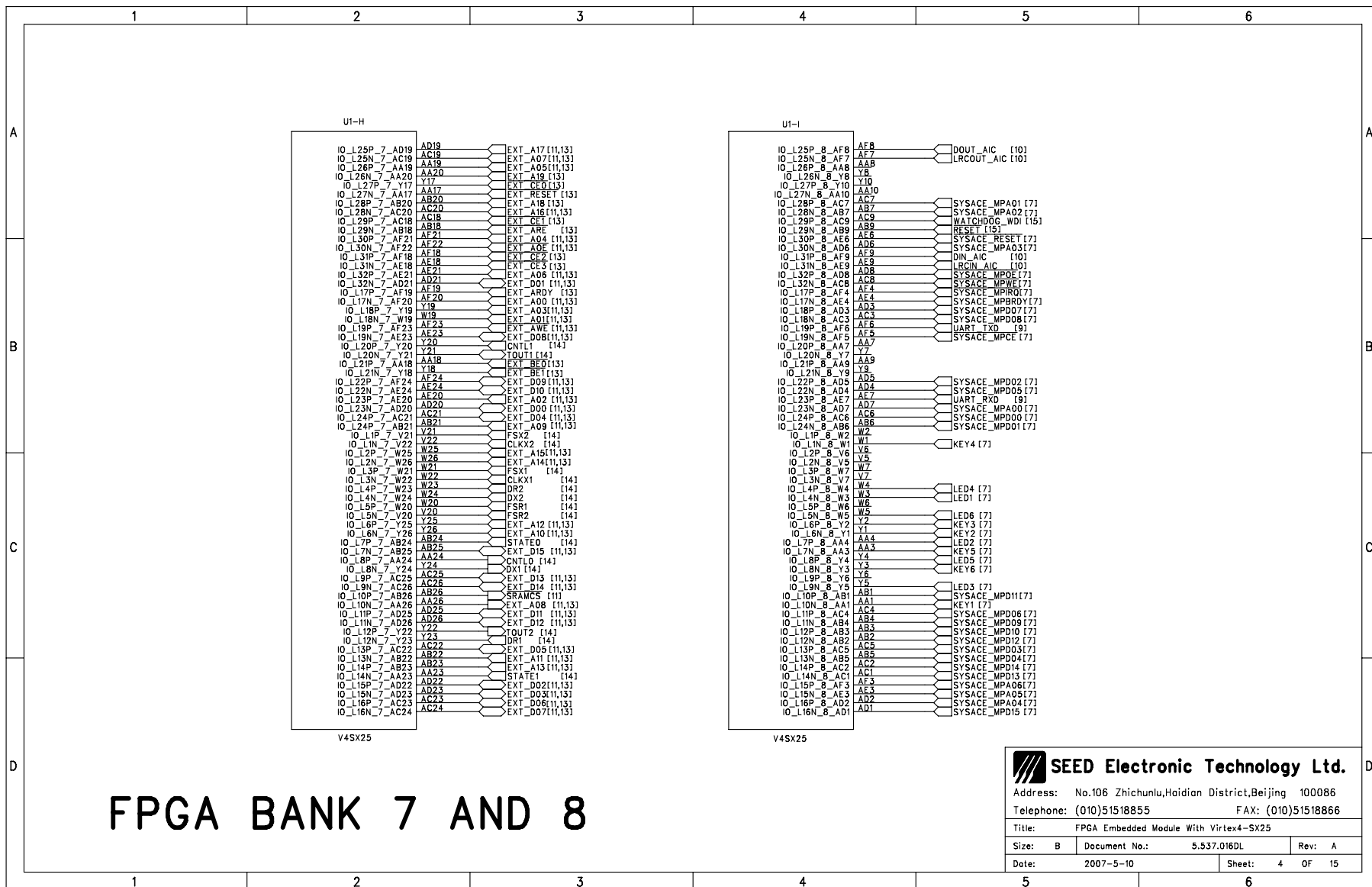




FPGA BANK 5 AND 6

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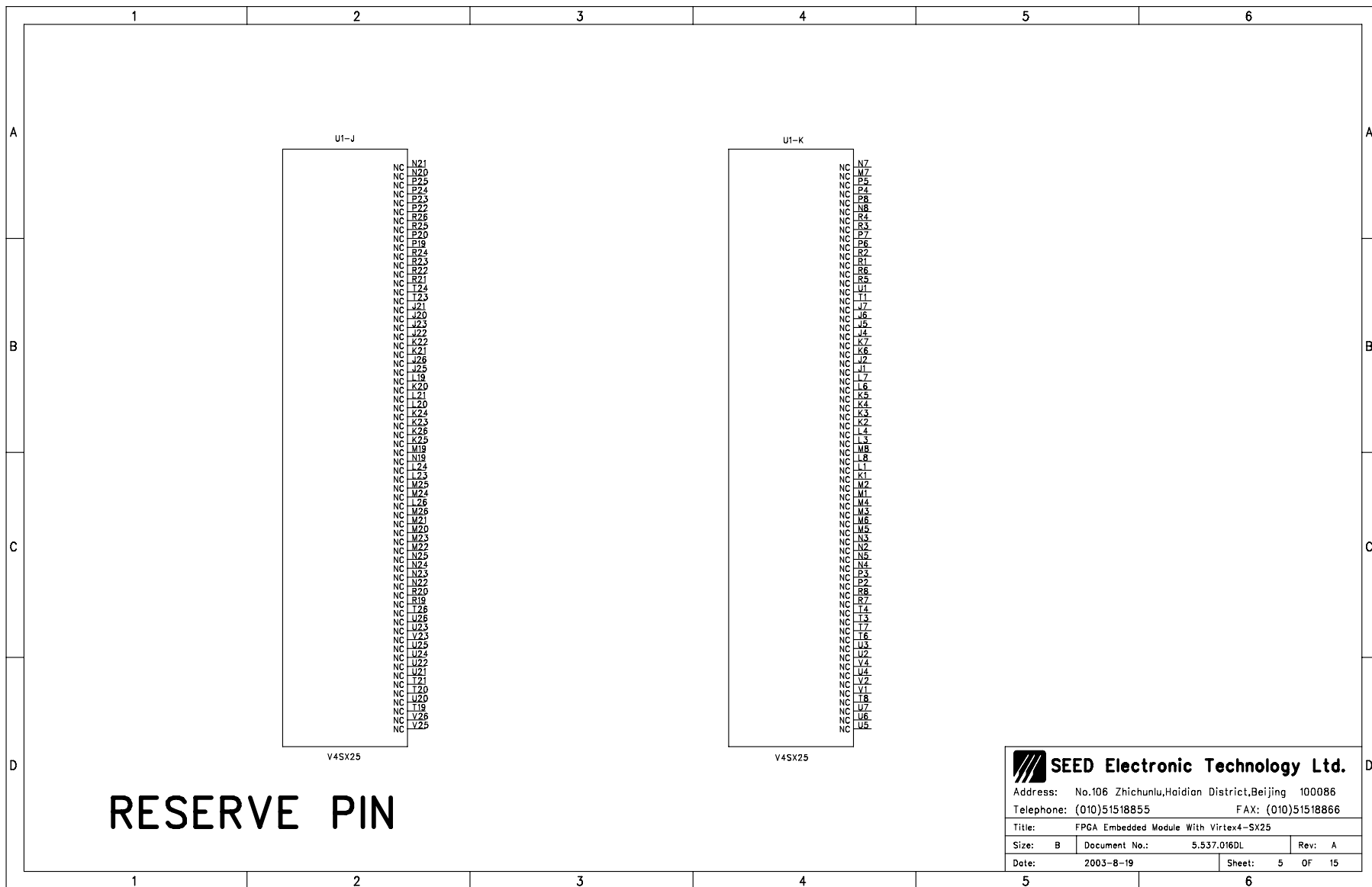
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| Title: FPGA Embedded Module With Virtex4-SX25 | | | |
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| Date: | 2007-5-10 | Sheet: 3 | OF 15 |

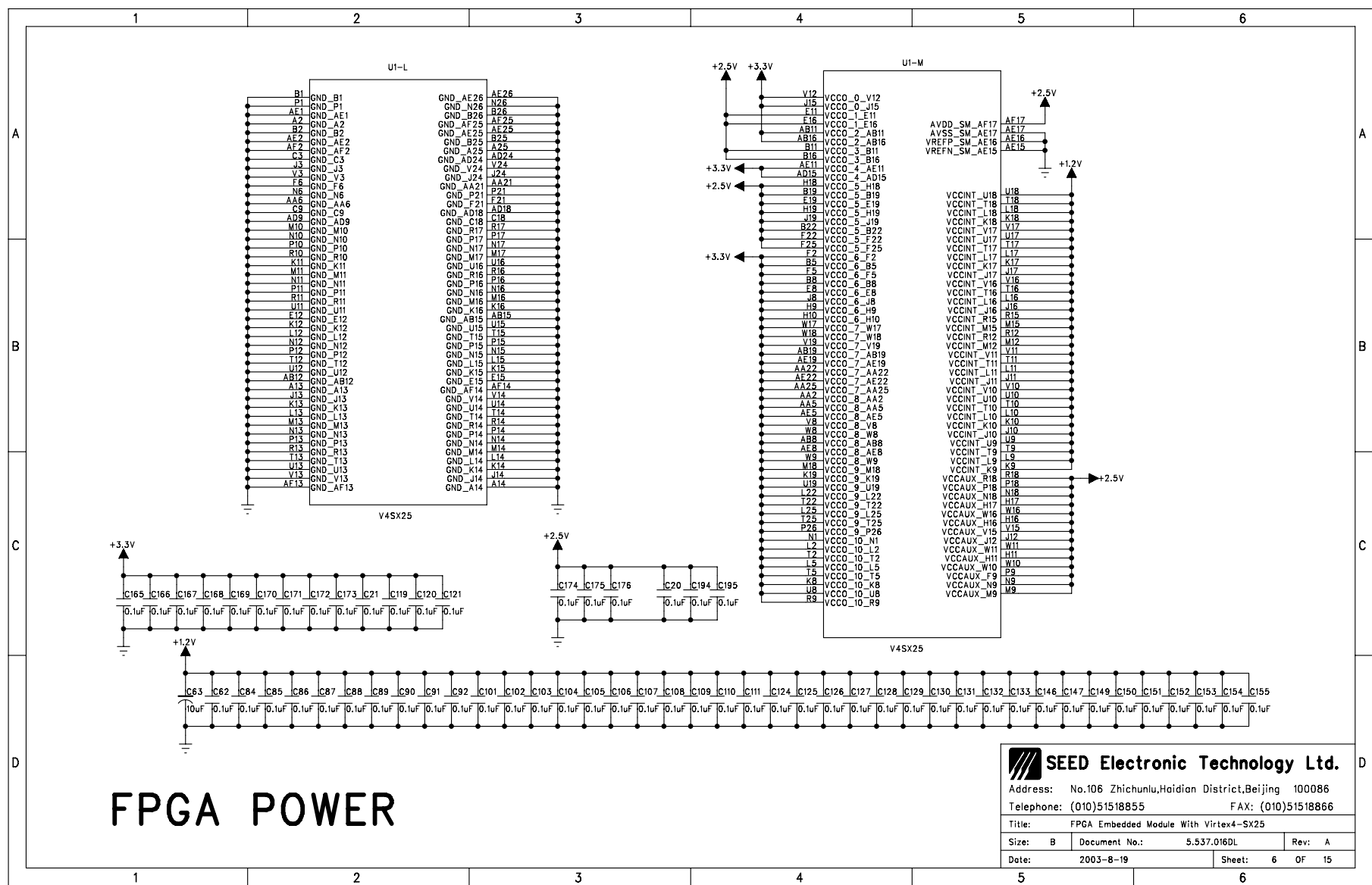


FPGA BANK 7 AND 8

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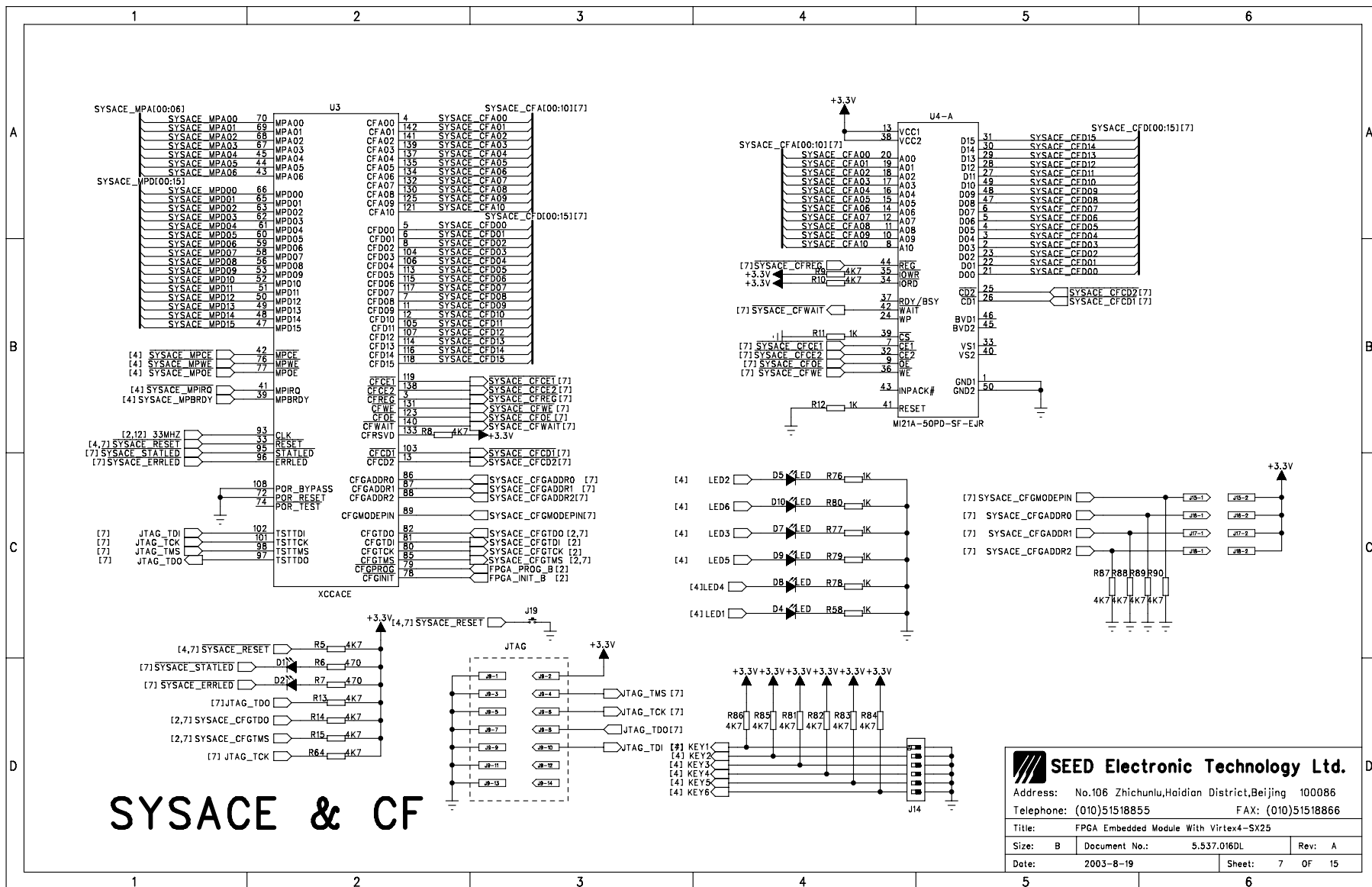
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| Title: FPGA Embedded Module With Virtex4-SX25 | | | |
| Size: B | Document No.: | 5.537.016DL | Rev: A |
| Date: | 2007-5-10 | Sheet: | 4 OF 15 |





FPGA POWER

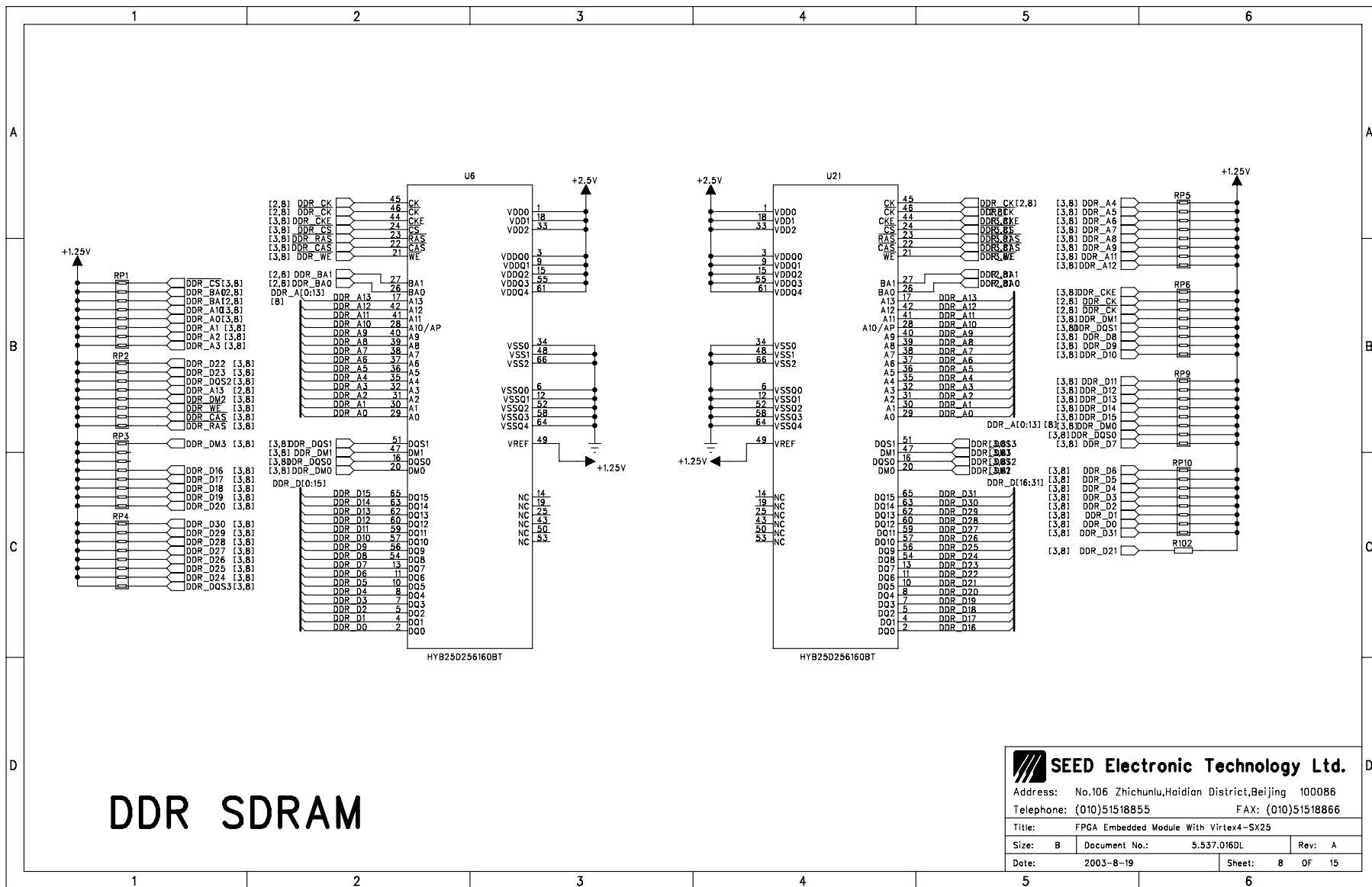
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| Title: FPGA Embedded Module With Virtex4-SX25 | | | |
| Size: B | Document No.: 5.537.016DL | Rev: A | |
| Date: 2003-8-19 | Sheet: 6 | OF 15 | |

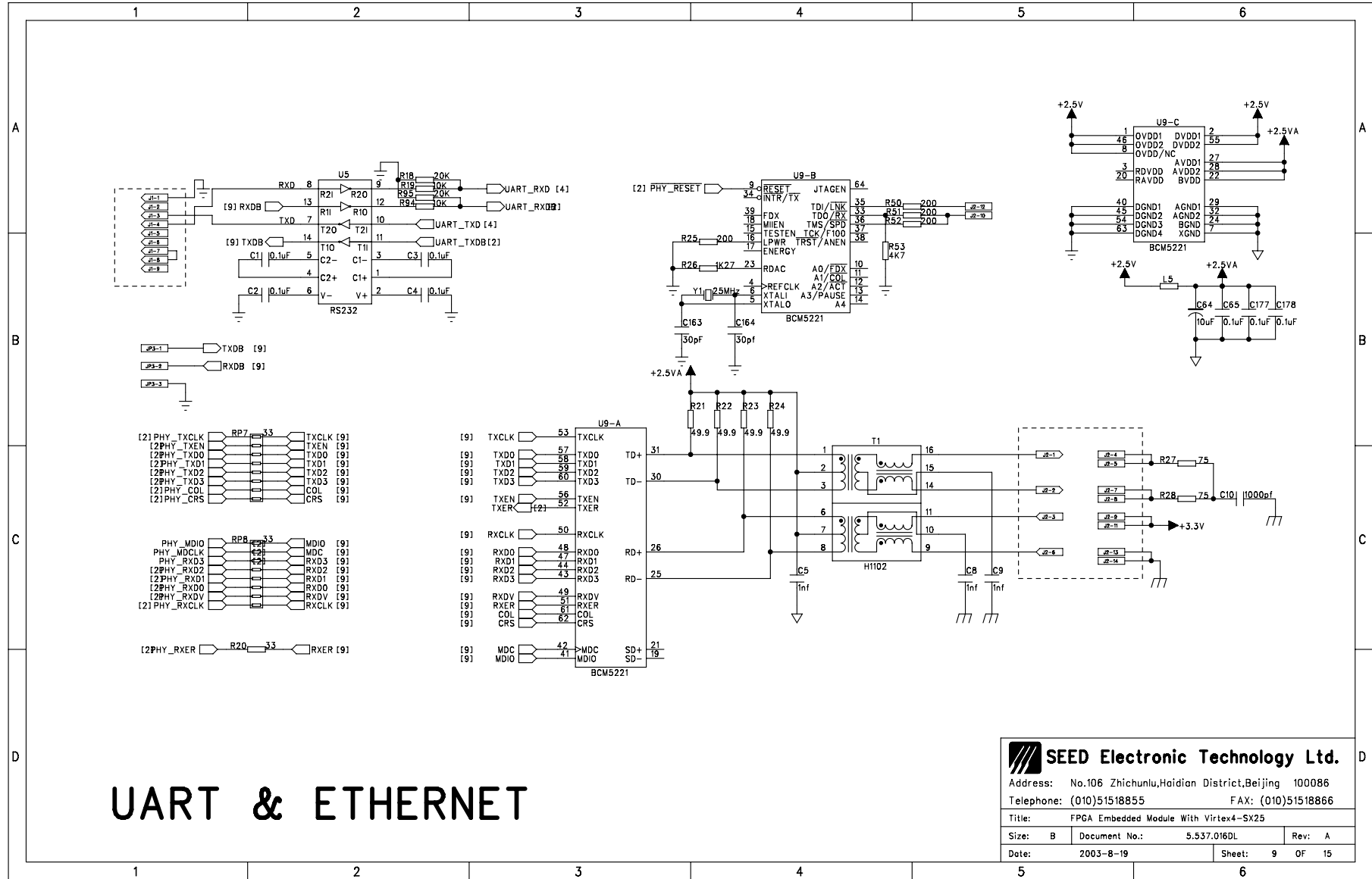


SYSACE & CF

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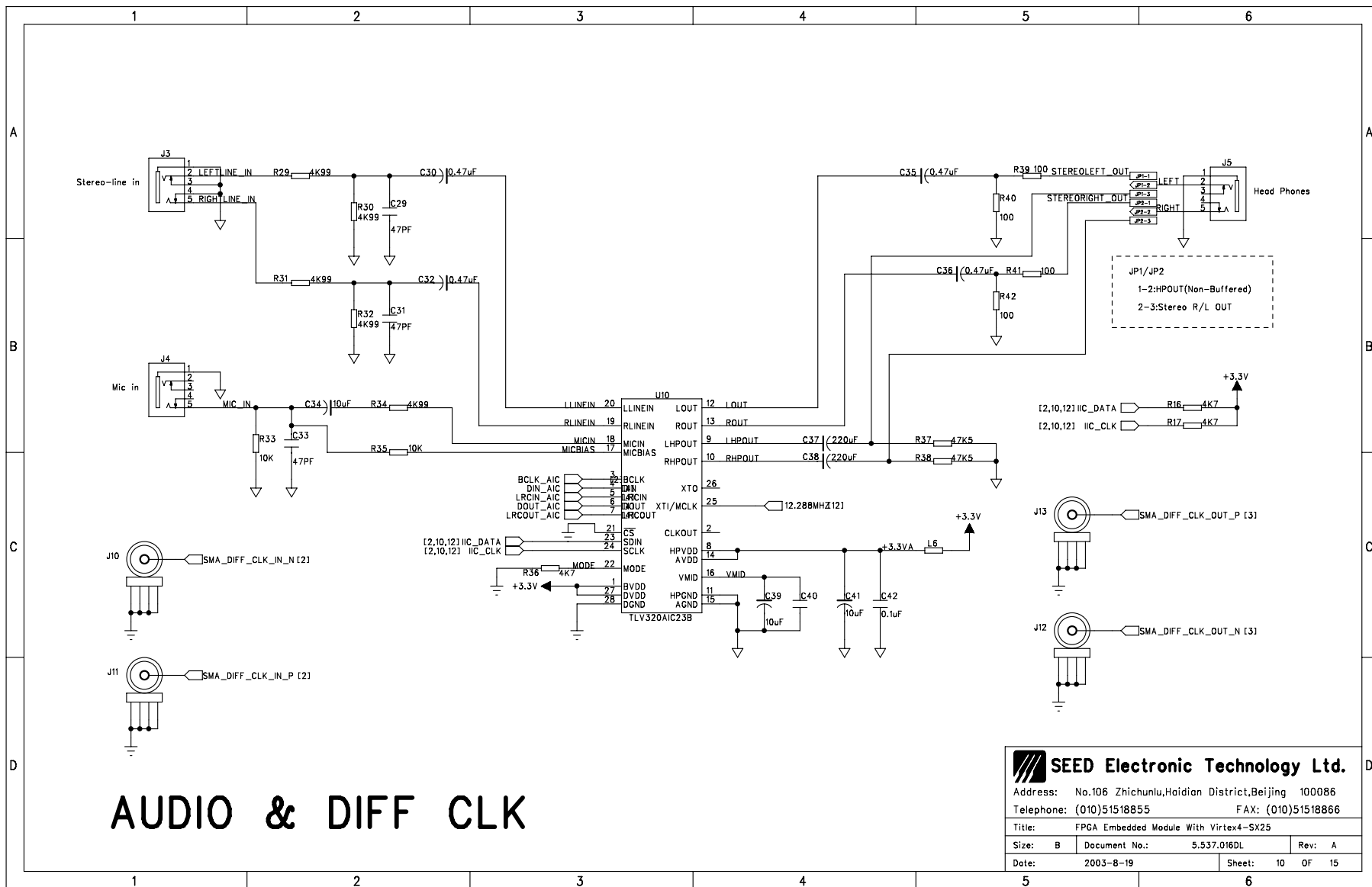
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| Size: B | Document No.: 5.537.016DL | Rev: A |
| Date: 2003-8-19 | Sheet: 7 OF 15 | |





UART & ETHERNET

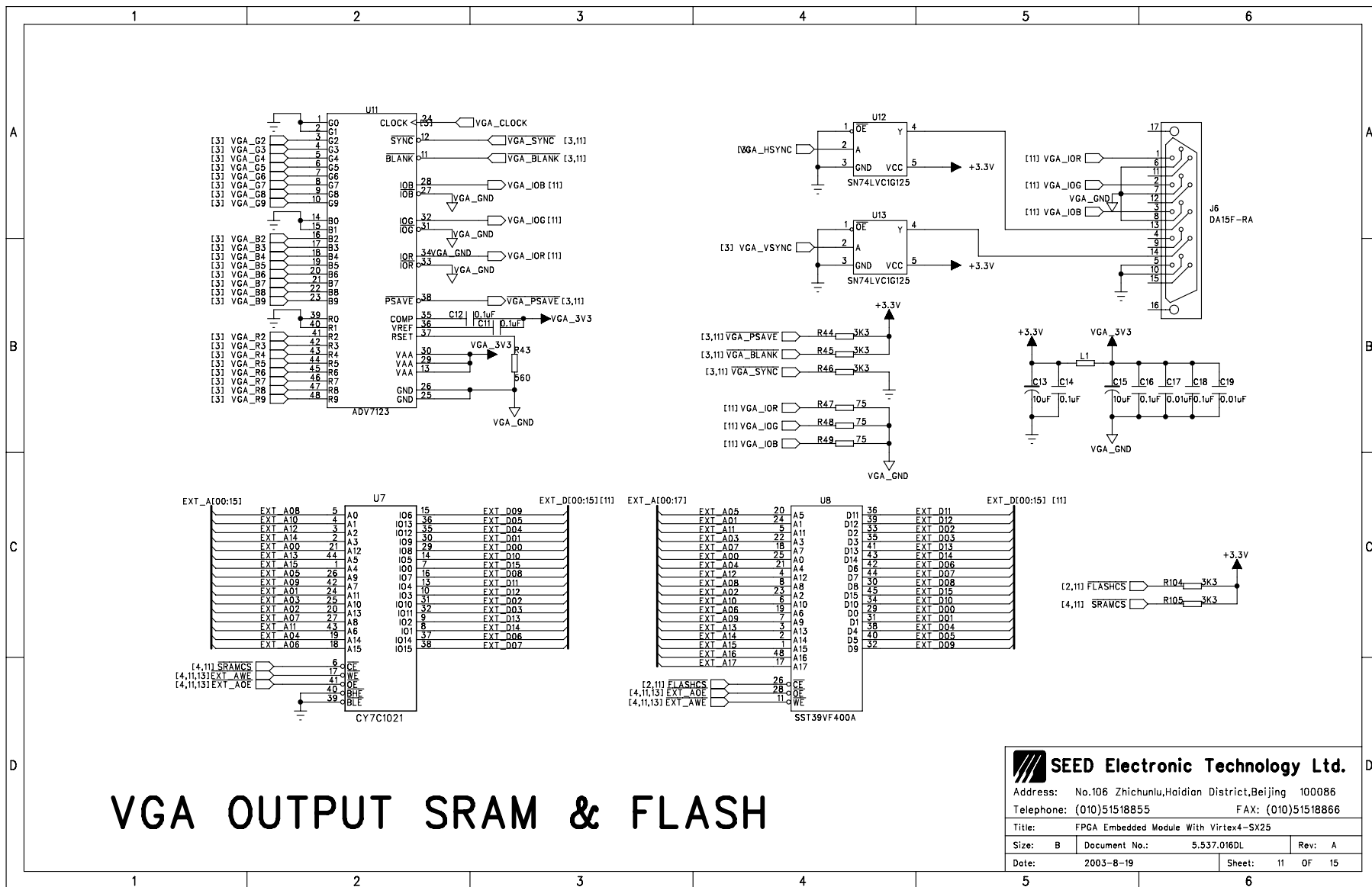
SEED Electronic Technology Ltd.
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 Title: FPGA Embedded Module With Virtex4-SX25
 Size: B Document No.: 5.537.016DL Rev: A
 Date: 2003-8-19 Sheet: 9 OF 15



AUDIO & DIFF CLK

SEED Electronic Technology Ltd.
 Address: No.106 Zhichunlu, Haidian District, Beijing 100086
 Telephone: (010)51518855 FAX: (010)51518866

| | | |
|---|---------------------------|--------|
| Title: FPGA Embedded Module With Virtex4-SX25 | | |
| Size: B | Document No.: 5.537.016DL | Rev: A |
| Date: 2003-8-19 | Sheet: 10 | OF 15 |



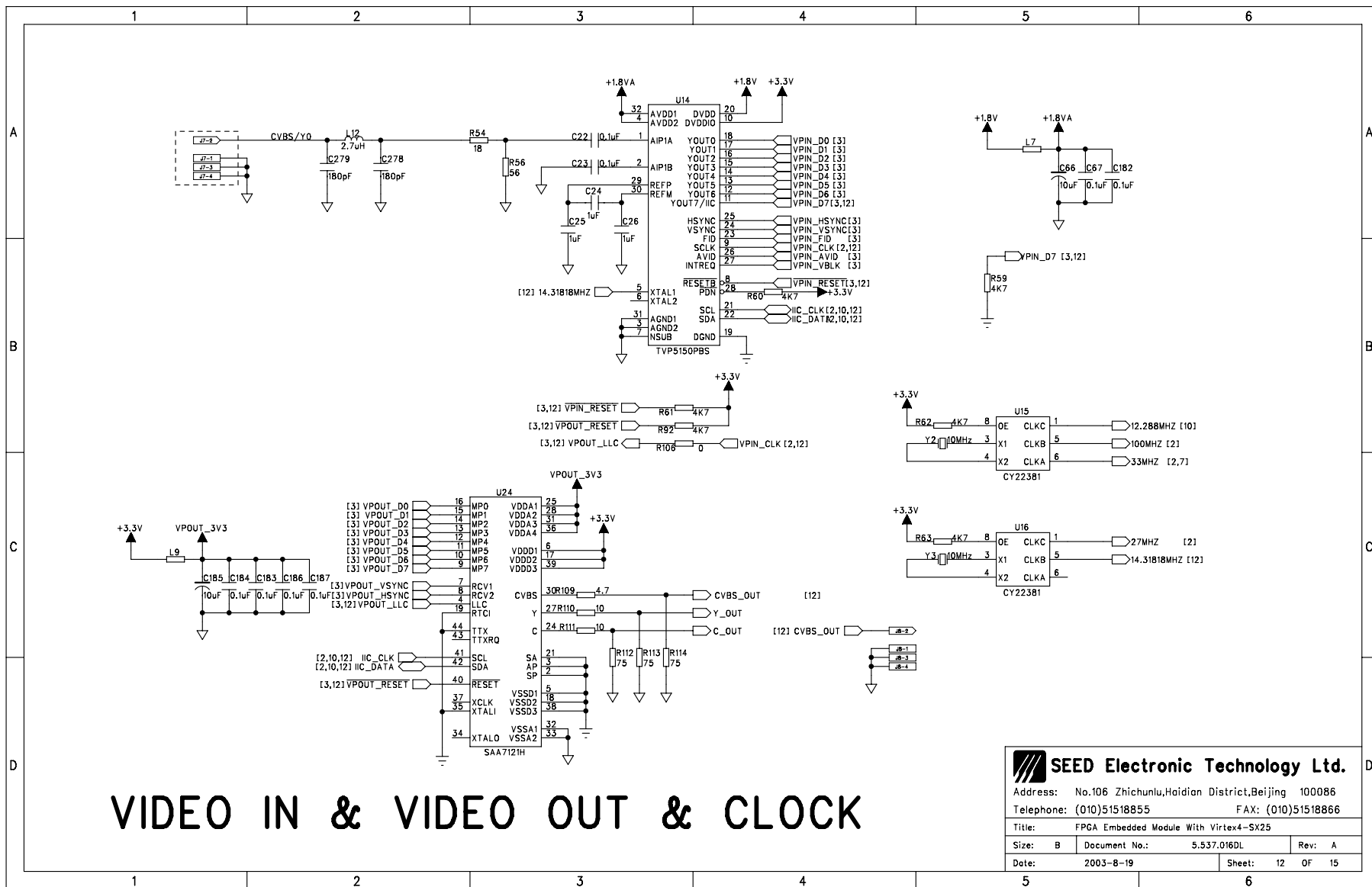
VGA OUTPUT SRAM & FLASH

SEED Electronic Technology Ltd.

Address: No.106 Zhichunlu, Haidian District, Beijing 100086
 Telephone: (010)51518855 FAX: (010)51518866

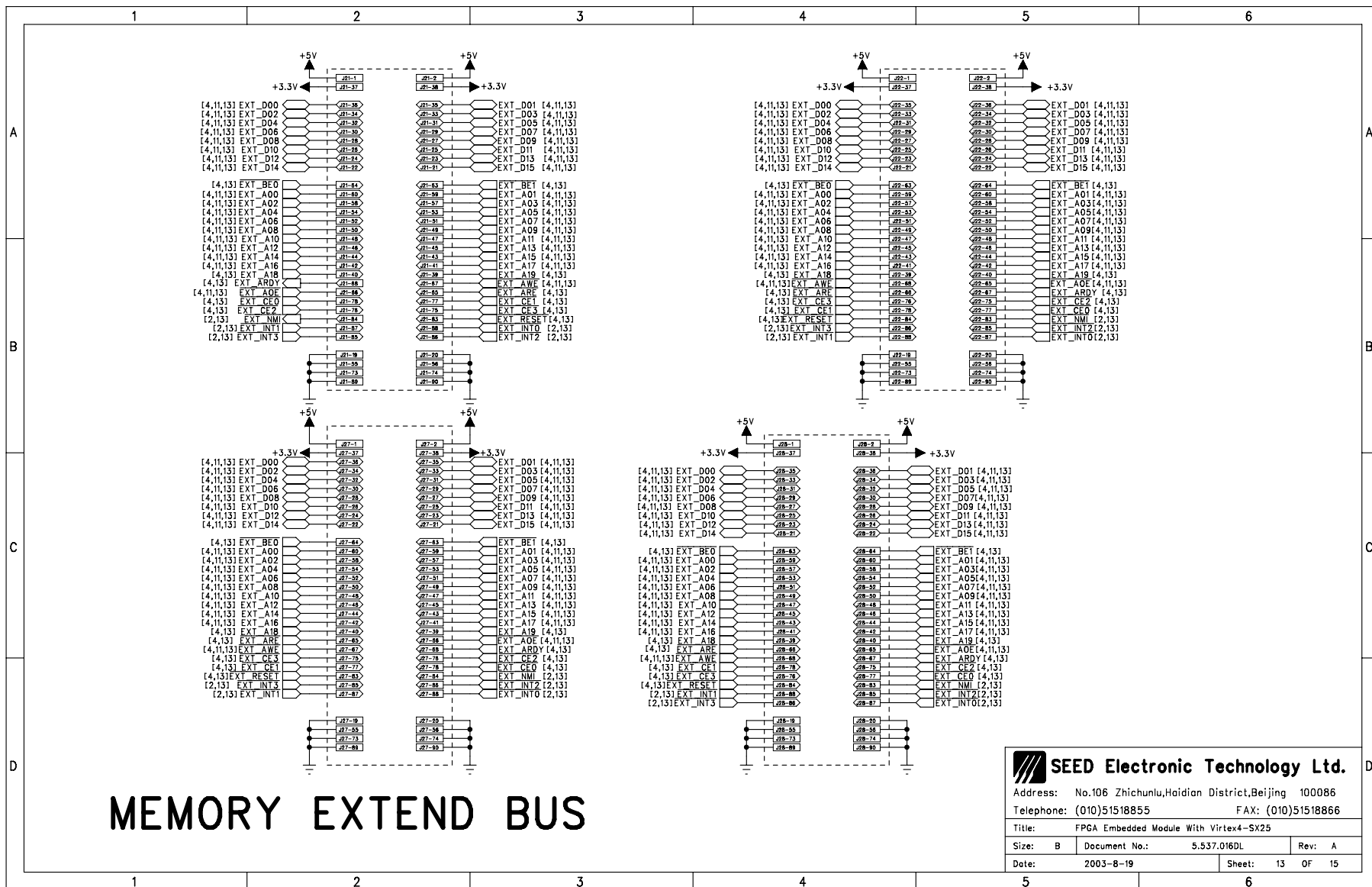
Title: FPGA Embedded Module With Virtex4-SX25

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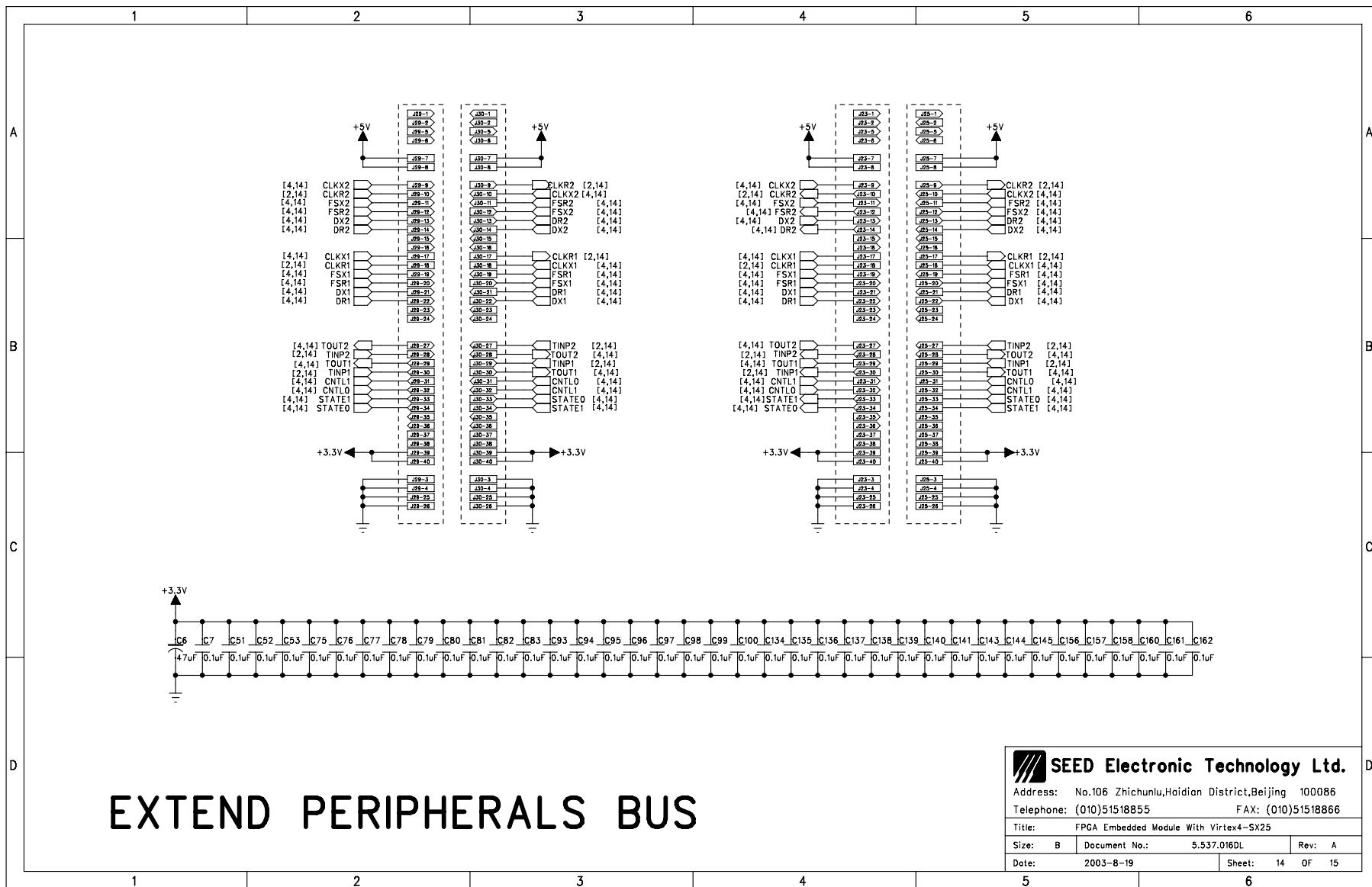
VIDEO IN & VIDEO OUT & CLOCK

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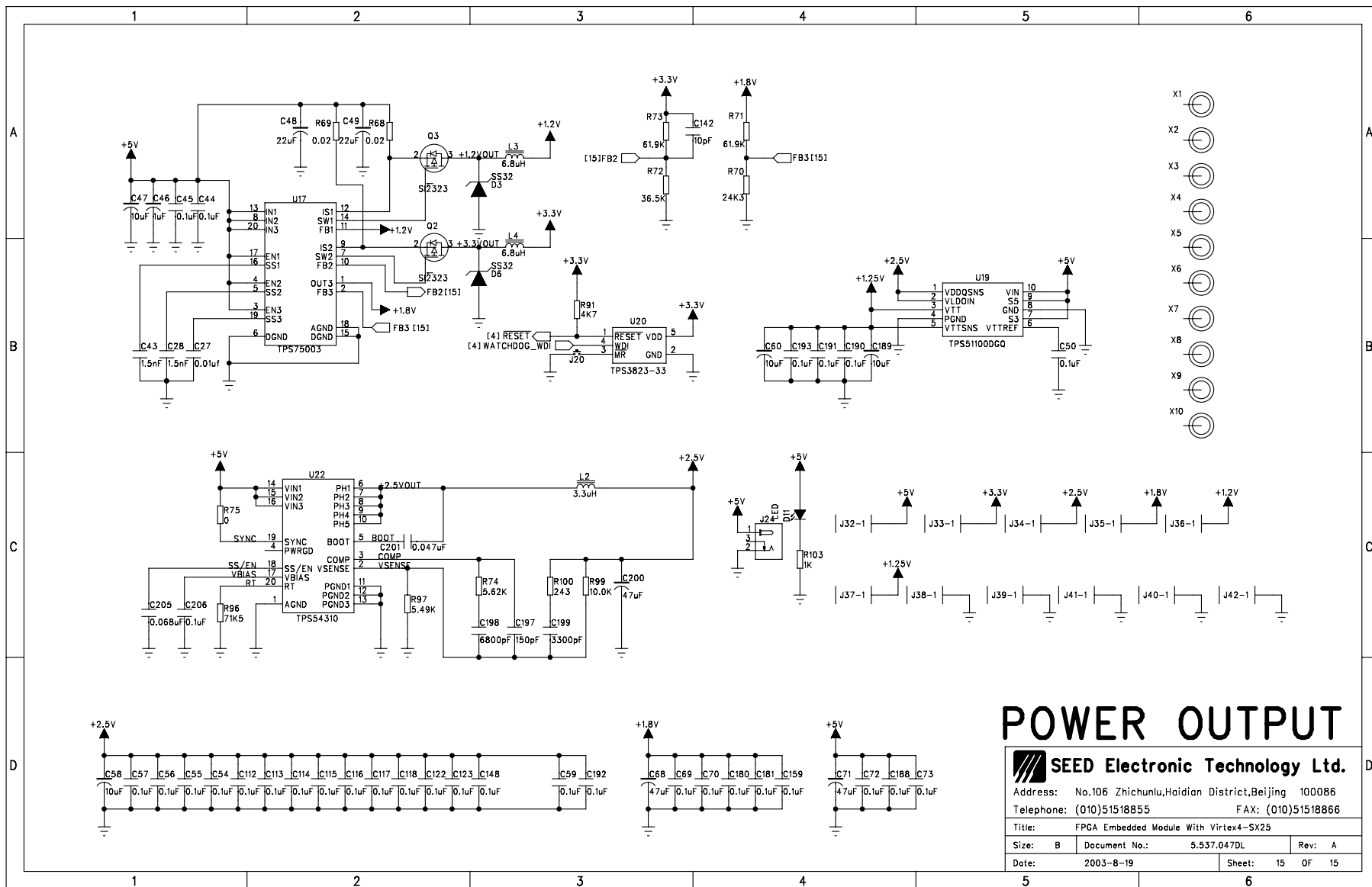
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EXTEND PERIPHERALS BUS

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POWER OUTPUT

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